19-3165; Rev 0; 1/04

EVALUATION KIT AVAILABLE

MAXIM

Dual, Interleaved, Fixed-Frequency Step-Down Controller with a Dynamically Adjustable Output

General Description

The MAX1549 dual pulse-width modulation (PWM) step-down controller provides the high efficiency, excellent transient response, and high DC-output accuracy necessary for generating low-voltage chipset and RAM power supplies in notebook computers. The controller employs a fixed-frequency, current-mode PWM architecture that does not require complex compensation. The MAX1549 also interleaves the dual step-down regulators, minimizing the input capacitor requirements.

The MAX1549 features differential current-sense inputs for accurately sensing the inductor current across an external current-sense resistor in series with the output to ensure reliable overload protection. Alternatively, the controller can provide overload protection using lossless inductor current-sensing methods, lowering power dissipation and reducing system cost.

Single-stage buck conversion allows the MAX1549 to directly step down high-voltage batteries for the highest possible efficiency. Very low output-voltage applications require two-stage conversion—stepping down from another system supply rail instead of the battery.

The MAX1549 powers chipsets and graphics processor cores that require dynamically adjustable output voltages, or generates the active termination bus that must track the input reference. The main step-down controller (OUT1) regulates the dedicated reference input (REFIN) voltage generated by a resistive voltage-divider from the MAX1549's reference. The MAX1549 also includes internal open-drain pulldowns with logic-level control inputs to dynamically adjust the REFIN resistive-divider ratio. When a transition occurs on these control inputs, the controller enters forced-PWM mode and blanks the power-good (PGOOD1) output and output fault protection. OUT2 uses a Dual-Mode™ feedback input to provide either fixed 2.5V/1.8V or adjustable output voltage regulation. The MAX1549 is available in a 40-pin, 6mm x 6mm thin QFN package.

Applications

Notebook Computers

Dynamically Adjustable Chipset Supplies

Video/GPU Core Supplies

DDR Memory Termination

CPU Core or V_{CC} Supplies

Fixed Chipset/RAM Supplies

Active Termination Buses

Dual Mode is a trademark of Maxim Integrated Products, Inc.

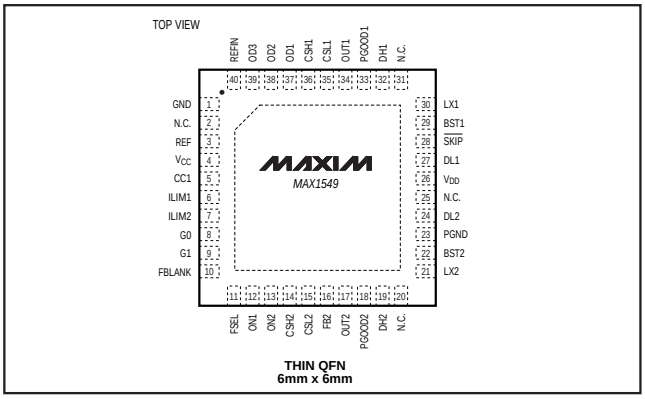
Features

- **Interleaved, Fixed-Frequency, Current-Mode Control Architecture**
- **1% V_{OUT} Accuracy Over Line and Load**
- **Main Output (OUT1)**
  - **0.5V to 2.0V Adjustable Output**
  - **External Reference Input for Dynamically Selectable Output Voltages**
  - **Four Digitally Selectable Output Voltages**
  - **Power-Good and Fault Blanking During Transitions**
- **Second Output (OUT2)**
  - **2.5V/1.8V Fixed or 0.5V to 2.7V Adjustable Output**
- **Accurate Differential Current-Sense Inputs**
- **100kHz/200kHz/300kHz/400kHz Selectable Switching Frequency**
- **Output Overvoltage/Undervoltage Protection**
- **Soft-Start and Soft-Shutdown**
- **Drives Large Synchronous-Rectifier FETs**
- **2V ±0.6% Reference Output**
- **Separate Enable Inputs with Accurate Threshold Voltages**
- **Separate Power-Good Window Comparators**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX1549ETL	-40°C to +85°C	40 Thin QFN 6mm x 6mm

Pin Configuration



THIN QFN
6mm x 6mm

Dual, Interleaved, Fixed-Frequency Step-Down Controller with a Dynamically Adjustable Output

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .....-0.3V to +6V
V_{DD} to PGND .....-0.3V to +6V
CSH_, CSL_, OUT_, PGOOD_, OD_ to GND .....-0.3V to (V_{CC} + 0.3V)
G0, G1, ILIM_, REFIN to GND .....-0.3V to +6V
FB2, $\overline{SKIP}$, ON_ to GND .....-0.3V to +6V
REF, CC1, FBLANK, FSEL to GND.....-0.3V to (V_{CC} + 0.3V)
DL1, DL2 to PGND .....-0.3V to (V_{DD} + 0.3V)
BST1, BST2 to PGND .....-0.3V to +36V
LX1 to BST1.....-6V to +0.3V
DH1 to LX1 .....-0.3V to (V_{BST1} + 0.3V)
LX2 to BST2.....-6V to +0.3V
DH2 to LX2 .....-0.3V to (V_{BST2} + 0.3V)
GND to PGND .....-0.3V to +0.3V
REF Short Circuit to GND .....Continuous
Continuous Power Dissipation (T_A = +70°C)
40-Pin 6mm x 6mm Thin QFN (derated 26.3mW/°C above +70°C).....2105mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V_{CC} = V_{DD} = 5V, $\overline{SKIP}$ = GND, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
INPUT SUPPLIES (Note 1)							
Input Voltage Range	V_{BIAS}	V_{CC}, V_{DD}		4.5		5.5	V
Quiescent Supply Current (V_{CC})	I_{CC}	OUT1 and FB2 forced above their regulation points			1.0	1.8	mA
Quiescent Supply Current (V_{DD})	I_{DD}	OUT1 and FB2 forced above their regulation points			1.5	5	µA
Shutdown Supply Current (V_{CC})		ON1 = ON2 = GND, $\overline{SKIP}$ = V_{CC}			2.5	5	µA
Shutdown Supply Current (V_{DD})		ON1 = ON2 = GND			<1	5	µA
PWM CONTROLLERS							
Main Output-Voltage Accuracy (OUT1 Tracking)	V_{REFIN} - V_{OUT1}	With respect to REFIN, $\overline{SKIP}$ = V_{CC} or GND	50% duty cycle	-5	0	+5	mV
			10% to 90% duty cycle	-10		+10	
Secondary Preset Output-Voltage Accuracy (OUT2 Fixed)	V_{OUT2}	$\overline{SKIP}$ = V_{CC}, 50% duty cycle (Note 1)	FB2 = GND	2.475	2.5	2.525	V
			FB2 = V_{CC}	1.780	1.8	1.820	
Secondary Feedback-Voltage Accuracy (FB2 Adjustable)	V_{FB2}	$\overline{SKIP}$ = V_{CC} (Note 1)	50% duty cycle	0.490	0.50	0.510	V
			10% to 90% duty cycle	0.485		0.515	
Load-Regulation Error		I_{LOAD} = 0 to 3A, $\overline{SKIP}$ = V_{CC}			0.1		%
V_{IN} Line-Regulation Error		V_{IN} = 2V to 28V			1		%
Output Adjust Range		OUT1 (tracks REFIN)		0.5		2.0	V
		OUT2		0.5		2.7	
OUT1 Input Bias Current	I_{OUT1}	V_{OUT1} = 0.5V to 2.0V		-1		+1	µA
FB2 Input Bias Current	I_{FB2}	V_{FB2} = 0 to 2.7V		-0.1		+0.1	µA
OUT2 Input Resistance	R_{OUT2}	FB2 = GND or adjustable		120	250	460	kΩ
		FB2 = V_{CC}		85	180	335	

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{CC} = V_{DD} = 5V, $\overline{SKIP}$ = GND, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
OUT_ Discharge-Mode On-Resistance	$R_{DISCHARGE}$				12	40	Ω
OUT_ Synchronous-Rectifier Discharge-Mode Turn-On Level				0.2	0.3	0.4	V
Operating Frequency	f_{OSC}	(Note 2)	FSEL = GND	70	100	130	kHz
			FSEL = REF	170	200	230	
			FSEL = open	270	300	330	
			FSEL = V_{CC}	350	400	450	
Minimum On-Time	$t_{ON(MIN)}$	(Note 3)				200	ns
Maximum Duty Cycle	D_{MAX}			91	93		%
Soft-Start Ramp Time	t_{SS}	Measured from the rising edge of ON_ to full scale			512 / f_{OSC}		s
REFERENCE (REF)							
Reference Voltage	V_{REF}	V_{CC} = 4.5V to 5.5V, I_{REF} = 0	T_A = +25°C	1.988	2.00	2.012	V
			T_A = 0°C to +85°C	1.985	2.00	2.015	
Reference Load Regulation	ΔV_{REF}	I_{REF} = -10µA to +100µA		1.980		2.020	V
REF Lockout Voltage	$V_{REF(UVLO)}$	Rising edge, hysteresis = 350mV			1.95		V
REFIN Voltage Range	V_{REFIN}			0.5		2.0	V
REFIN Input Bias Current	I_{REFIN}			-50		+50	nA
FAULT DETECTION							
Output Overvoltage Trip Threshold		With respect to error-comparator threshold		12	14.5	17	%
Output Overvoltage Fault-Propagation Delay	t_{OVP}	OUT1 and FB2 forced 2% above trip threshold			10		µs
Output Undervoltage-Protection Trip Threshold		With respect to error-comparator threshold		65	70	75	%
Output Undervoltage-Protection Blanking Time	t_{BLANK}	From rising edge of ON_			4096 / f_{OSC}		s
Output Undervoltage Fault-Propagation Delay	t_{UVP}				10		µs
PGOOD_ Lower Trip Threshold		With respect to error-comparator threshold, hysteresis = 1%		-12.5	-10	-7.5	%
PGOOD_ Upper Trip Threshold		With respect to error-comparator threshold, hysteresis = 1%		+7.5	+10	+12.5	%
PGOOD_ Propagation Delay	$t_{PGOOD\_}$	OUT1 and FB2 forced 2% beyond PGOOD_ trip threshold			10		µs
PGOOD_ Output Low Voltage		I_{SINK} = 4mA				0.3	V
PGOOD_ Leakage Current	$I_{PGOOD\_}$	OUT1 = REFIN and V_{FB2} = 0.5V (PGOOD_ high impedance), PGOOD_ forced to 5.5V				1	µA

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{CC} = V_{DD} = 5V, $\overline{SKIP}$ = GND, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Fault-Blanking Time	t_{FBLANK}	FBLANK = V_{CC}		110	150	190	µs
		FBLANK = open		60	100	140	
		FBLANK = REF		22	50	75	
Thermal-Shutdown Threshold	T_{SHDN}	Hysteresis = 15°C			+165		°C
V_{CC} Undervoltage-Lockout Threshold	$V_{CC(UVLO)}$	Rising edge, PWM disabled below this level, hysteresis = 50mV		4.1	4.25	4.4	V
CURRENT LIMIT							
ILIM_ Adjustment Range				0.25		V_{REF}	V
Current-Limit Input Range		$V_{CSH\_}$, $V_{CSL\_}$		0		2.7	V
CSH_/CSL_ Input Bias Current		$V_{CSH\_}$ = $V_{CSL\_}$ = 0 to 2.7V		-0.15		+0.15	µA
Current-Limit Threshold (Fixed)	V_{LIMIT}	$V_{CSH\_}$ - $V_{CSL\_}$, ILIM_ = V_{CC}		65	70	75	mV
Current-Limit Threshold (Adjustable)	V_{LIMIT}	$V_{CSH\_}$ - $V_{CSL\_}$	$V_{ILIM\_}$ = 2.0V	170	200	230	mV
			$V_{ILIM\_}$ = 1.0V	91	100	109	
			$V_{ILIM\_}$ = 0.5V	42	50	58	
Current-Limit Threshold (Zero Crossing)	V_{ZX}	V_{PGND} - $V_{LX\_}$, $\overline{SKIP}$ = GND			3		mV
Idle-Mode™ Threshold		$V_{CSH\_}$ - $V_{CSL\_}$	ILIM_ = V_{CC}	10	15	20	mV
			With respect to current-limit threshold		20		%
ILIM_ Leakage Current				-0.1		+0.1	µA
GATE DRIVERS							
DH_ Gate-Driver On-Resistance	R_{DH}	BST_ - LX_ forced to 5V			1.5	6	Ω
DL_ Gate-Driver On-Resistance	R_{DL}	DL_, high state			1.5	6	Ω
		DL_, low state			0.5	2.7	
DH_ Gate-Driver Source/Sink Current	I_{DH}	DH_ forced to 2.5V, BST_ - LX_ forced to 5V			1		A
DL_ Gate-Driver Source Current	$I_{DL (SOURCE)}$	DL_ forced to 2.5V			1		A
DL_ Gate-Driver Sink Current	$I_{DL (SINK)}$	DL_ forced to 2.5V			3		A
Dead Time	t_{DEAD}	DL_ rising			35		ns
		DH_ rising			26		
INPUTS AND OUTPUTS							
OD_ On-Resistance	$R_{OD\_}$				10	100	Ω
OD_ Leakage Current	$I_{OD\_}$	OD_ high impedance, $V_{OD\_}$ = 5.5V				100	nA
ON_ Logic Input Threshold		Rising edge, hysteresis = 600mV		2.4	2.6	2.8	V
Logic Input Voltage		$\overline{SKIP}$, G0, G1 hysteresis = 600mV	High	2.4			V
			Low			0.8	

Idle Mode is a trademark of Maxim Integrated Products, Inc.

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{CC} = V_{DD} = 5V, $\overline{SKIP}$ = GND, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Logic Input Current		ON_, $\overline{SKIP}$, G0, G1		-1		+1	µA
Dual-Mode Threshold Voltage		FB2	High	1.9	2.0	2.1	V
			Low	0.05	0.1	0.15	
Four-Level Input Logic Levels		FSEL, FBLANK	High	V_{CC} - 0.4V			V
			Open	3.15		3.85	
			REF	1.65		2.35	
			Low			0.5	
Four-Level Logic Input Current		FSEL, FBLANK forced to GND or V_{CC}		-3		+3	µA

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V_{CC} = V_{DD} = 5V, $\overline{SKIP}$ = GND, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS		MIN	MAX	UNITS
INPUT SUPPLIES (Note 1)						
Input Voltage Range	V_{BIAS}	V_{CC}, V_{DD}		4.5	5.5	V
Quiescent Supply Current (V_{CC})	I_{CC}	OUT1 and FB2 forced above their regulation points			1.8	mA
Quiescent Supply Current (V_{DD})	I_{DD}	OUT1 and FB2 forced above their regulation points			5	µA
Shutdown Supply Current (V_{CC})		ON1 = ON2 = GND, $\overline{SKIP}$ = V_{CC}			5	µA
Shutdown Supply Current (V_{DD})		ON1 = ON2 = GND			5	µA
PWM CONTROLLERS						
Main Output-Voltage Accuracy (OUT1 Tracking)	V_{REFIN} - V_{OUT1}	With respect to REFIN, $\overline{SKIP}$ = V_{CC} or GND	50% duty cycle	-8	+8	mV
			10% to 90% duty cycle	-10	+10	
Secondary Preset Output-Voltage Accuracy (OUT2 Fixed)	V_{OUT2}	$\overline{SKIP}$ = V_{CC}, 50% duty cycle (Note 1)	FB2 = GND	2.470	2.530	V
			FB2 = V_{CC}	1.775	1.825	
Secondary Feedback-Voltage Accuracy (FB2 Adjustable)	V_{FB2}	$\overline{SKIP}$ = V_{CC} (Note 1)	50% duty cycle	0.490	0.510	V
			10% to 90% duty cycle	0.485	0.515	
Output Adjust Range		OUT1 (tracks REFIN)		0.5	2.0	V
		OUT2		0.5	2.7	
OUT2 Input Resistance	R_{OUT2}	FB2 = GND or adjustable		120	460	kΩ
		FB2 = V_{CC}		85	335	
OUT_ Discharge-Mode On-Resistance	$R_{DISCHARGE}$				40	Ω
OUT_ Synchronous-Rectifier Discharge-Mode Turn-On Level				0.2	0.4	V

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{CC} = V_{DD} = 5V, $\overline{SKIP}$ = GND, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS		MIN	MAX	UNITS
Operating Frequency	f_{OSC}	(Note 2)	FSEL = GND	70	130	kHz
			FSEL = REF	170	230	
			FSEL = open	270	330	
			FSEL = V_{CC}	350	450	
Maximum Duty Cycle	D_{MAX}			91		%
REFERENCE (REF)						
Reference Voltage	V_{REF}	V_{CC} = 4.5V to 5.5V, I_{REF} = 0		1.985	2.015	V
Reference Load Regulation	ΔV_{REF}	I_{REF} = -10µA to +100µA		1.980	2.020	V
REFIN Voltage Range				0.5	2.0	V
FAULT DETECTION						
Output Overvoltage Trip Threshold		With respect to error-comparator threshold		12	17	%
Output Undervoltage-Protection Trip Threshold		With respect to error-comparator threshold		65	75	%
PGOOD_ Lower Trip Threshold		With respect to error-comparator threshold, hysteresis = 1%		-12.5	-7.5	%
PGOOD_ Upper Trip Threshold		With respect to error-comparator threshold, hysteresis = 1%		+7.5	+12.5	%
PGOOD_ Output Low Voltage		I_{SINK} = 4mA			0.3	V
Fault-Blanking Time	t_{FBLANK}	FBLANK = V_{CC}		110	190	µs
		FBLANK = open		60	140	
		FBLANK = REF		22	75	
V_{CC} Undervoltage-Lockout Threshold	$V_{CC(UVLO)}$	Rising edge, PWM disabled below this level, hysteresis = 50mV		4.1	4.4	V
CURRENT LIMIT						
ILIM_ Adjustment Range				0.25	V_{REF}	V
Current-Limit Input Range		$V_{CSH\_}$, $V_{CSL\_}$		0	2.7	V
Current-Limit Threshold (Fixed)	V_{LIMIT}	$V_{CSH\_}$ - $V_{CSL\_}$, ILIM_ = V_{CC}		65	75	mV
Current-Limit Threshold (Adjustable)	V_{LIMIT}	$V_{CSH\_}$ - $V_{CSL\_}$	$V_{ILIM\_}$ = 2.0V	170	230	mV
			$V_{ILIM\_}$ = 1.0V	89	111	
			$V_{ILIM\_}$ = 0.5V	42	58	
Idle-Mode Threshold		$V_{CSH\_}$ - $V_{CSL\_}$, ILIM_ = V_{CC}		10	20	mV
GATE DRIVERS						
DH_ Gate-Driver On-Resistance	R_{DH}	BST_ - LX_ forced to 5V			6	Ω
DL_ Gate-Driver On-Resistance	R_{DL}	DL_, high state			6	Ω
		DL_, low state			2.7	

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{CC} = V_{DD} = 5V, $\overline{SKIP}$ = GND, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS		MIN	MAX	UNITS
INPUTS AND OUTPUTS						
OD_ On-Resistance	$R_{OD\_}$				100	Ω
ON_ Logic Input Threshold		Rising edge, hysteresis = 600mV		2.4	2.8	V
Logic Input Voltage		$\overline{SKIP}$, G0, G1, hysteresis = 600mV	High	2.4		V
			Low		0.8	
Dual-Mode Threshold Voltage		FB2	High	1.9	2.1	V
			Low	0.05	0.15	
Four-Level Input Logic Levels		FSEL, FBLANK	High	V_{CC} - 0.4V		V
			Open	3.15	3.85	
			REF	1.65	2.35	
			Low		0.5	

Note 1: When the inductor is in continuous conduction, the output voltage has a DC regulation level lower than the error-comparator threshold by 50% of the ripple. In discontinuous conduction ($\overline{SKIP}$ = GND, light load), the output voltage has a DC regulation level higher than the trip level by approximately 1.5% due to slope compensation.

Note 2: The MAX1549 cannot operate over all combinations of frequency, input voltage (V_{IN}), and output voltage. For large input-to-output differentials and high switching-frequency settings, the required on-time may be too short to maintain the regulation specifications. Under these conditions, a lower operating frequency must be selected. The minimum on-time must be greater than 150ns, regardless of the selected switching frequency. On-time and off-time specifications are measured from the 50% point to the 50% point at the DH_ pin with LX_ = GND, $V_{BST\_}$ = 5V, and a 250pF capacitor connected from DH_ to LX_. Actual in-circuit times may differ due to MOSFET switching speeds.

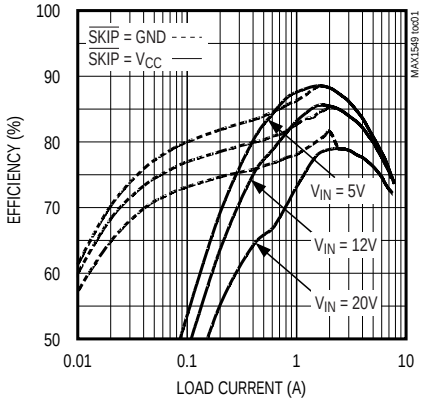
Note 3: Specifications are guaranteed by design, not production tested.

Note 4: Specifications to -40°C are guaranteed by design, not production tested.

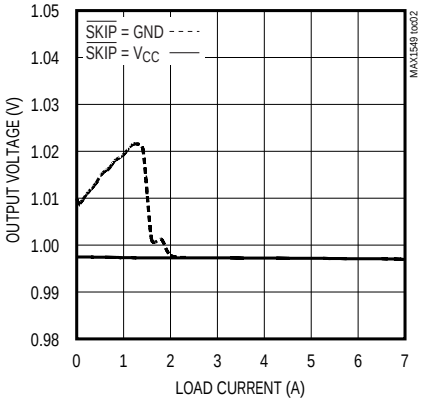
Typical Operating Characteristics

(MAX1549 circuit of Figure 1, V_{IN} = 12V, V_{DD} = V_{CC} = 5V, $\overline{SKIP}$ = GND, FSEL = open, T_A = +25°C, unless otherwise noted.)

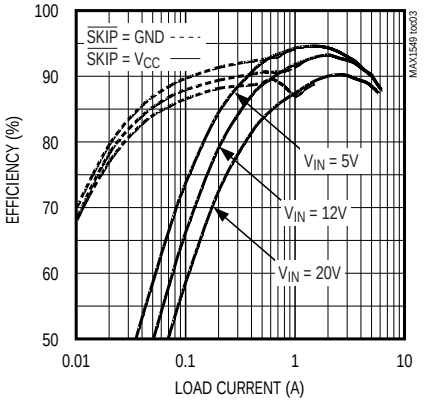
OUT1 EFFICIENCY vs. LOAD CURRENT (V_{OUT1} = 1.0V)



1.0V OUTPUT VOLTAGE (OUT1) vs. LOAD CURRENT



OUT2 EFFICIENCY vs. LOAD CURRENT (V_{OUT2} = 2.5V)

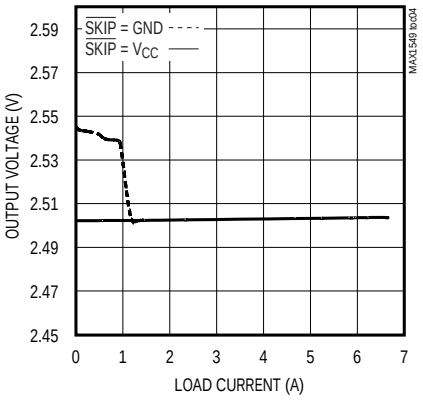


Dual, Interleaved, Fixed-Frequency Step-Down Controller with a Dynamically Adjustable Output

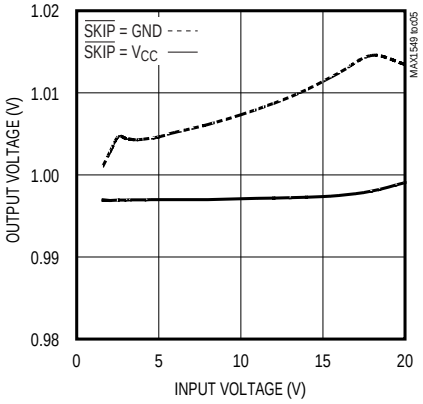
Typical Operating Characteristics (continued)

(MAX1549 circuit of Figure 1, V_{IN} = 12V, V_{DD} = V_{CC} = 5V, $\overline{SKIP}$ = GND, FSEL = open, T_A = +25°C, unless otherwise noted.)

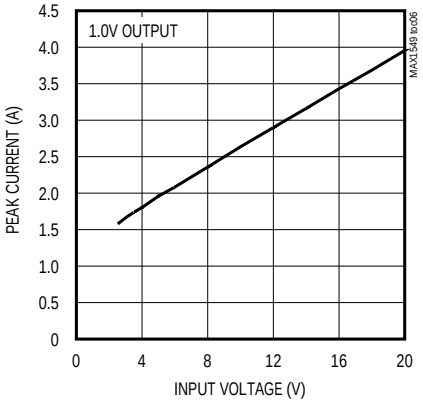
2.5V OUTPUT VOLTAGE (OUT2) vs. LOAD CURRENT



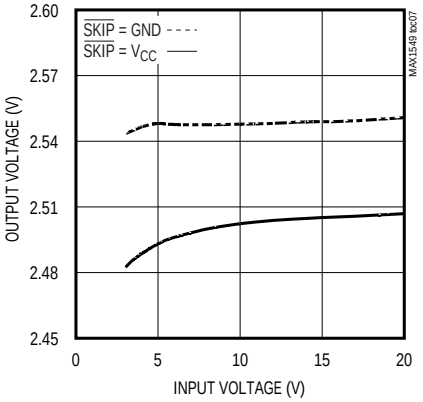
1.0V OUTPUT VOLTAGE (OUT1) vs. INPUT VOLTAGE



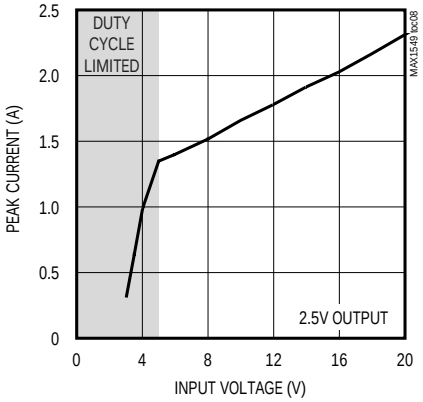
IDLE-MODE CURRENT vs. INPUT VOLTAGE



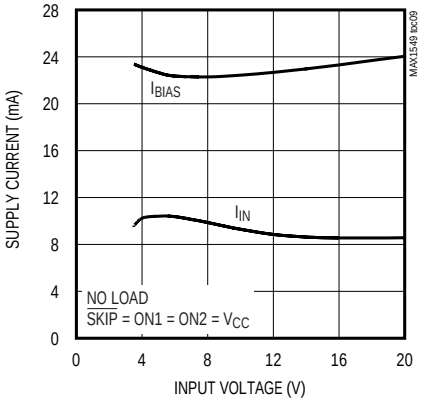
2.5V OUTPUT VOLTAGE (OUT2) vs. INPUT VOLTAGE



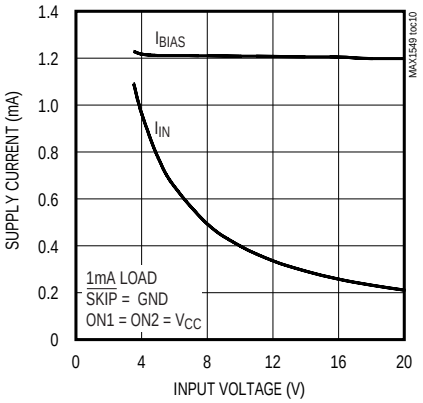
IDLE-MODE CURRENT vs. INPUT VOLTAGE



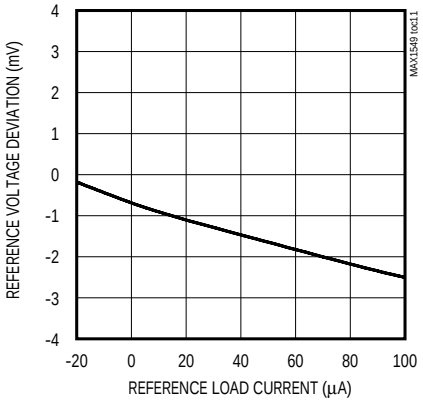
SUPPLY CURRENT vs. INPUT VOLTAGE (FORCED-PWM OPERATION)



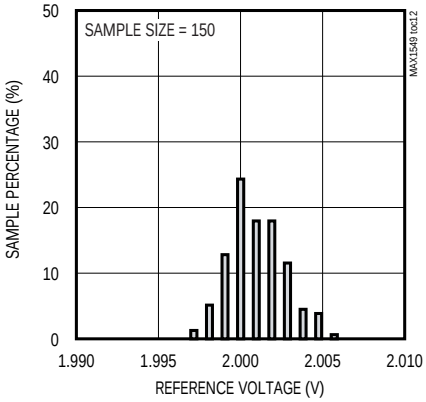
SUPPLY CURRENT vs. INPUT VOLTAGE (PULSE-SKIPPING OPERATION)



2.0V REFERENCE LOAD REGULATION



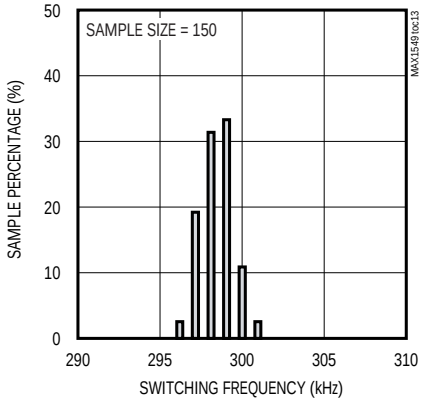
REFERENCE DISTRIBUTION



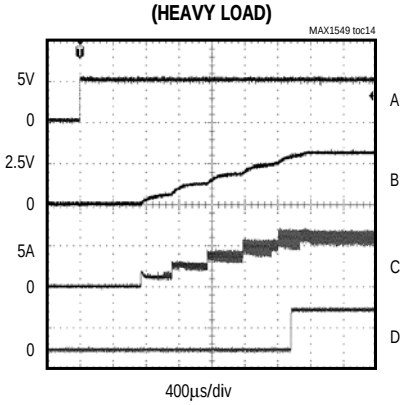
Typical Operating Characteristics (continued)

(MAX1549 circuit of Figure 1, V_{IN} = 12V, V_{DD} = V_{CC} = 5V, $\overline{SKIP}$ = GND, FSEL = open, T_A = +25°C, unless otherwise noted.)

SWITCHING FREQUENCY DISTRIBUTION (300kHz OPERATION)

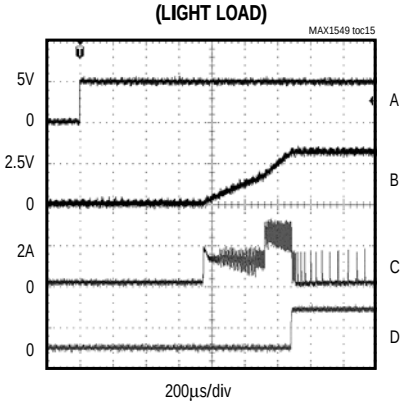


STARTUP WAVEFORM (HEAVY LOAD)



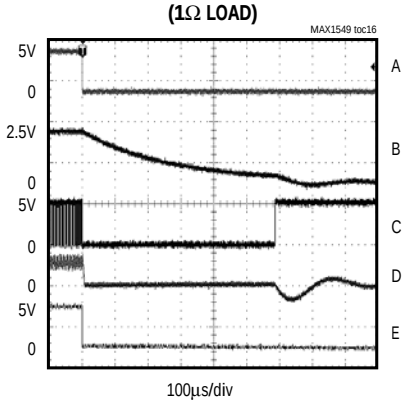
A: ON2, 5V/div
B: 2.5V OUTPUT, 2V/div
0.5Ω LOAD
C: INDUCTOR CURRENT, 5A/div
D: PGOOD2, 5V/div

STARTUP WAVEFORM (LIGHT LOAD)



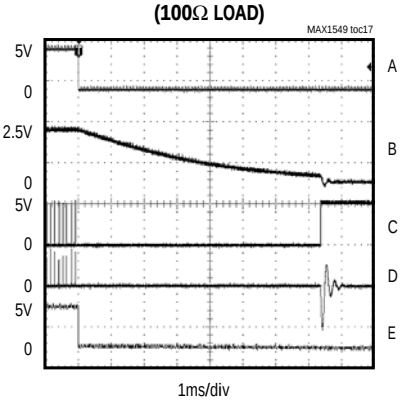
A: ON2, 5V/div
B: 2.5V OUTPUT, 2V/div
100Ω LOAD
C: INDUCTOR CURRENT, 2A/div
D: PGOOD2, 5V/div

SHUTDOWN WAVEFORM (1Ω LOAD)



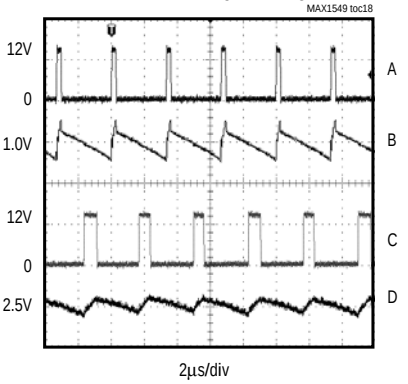
A: ON2, 5V/div
B: OUT2, 2V/div
C: DL2, 5V/div
D: INDUCTOR CURRENT, 5A/div
E: PGOOD2, 5V/div

SHUTDOWN WAVEFORM (100Ω LOAD)



A: ON2, 5V/div
B: OUT2, 2V/div
C: DL2, 5V/div
D: INDUCTOR CURRENT, 2A/div
E: PGOOD2, 5V/div

INTERLEAVED OPERATION



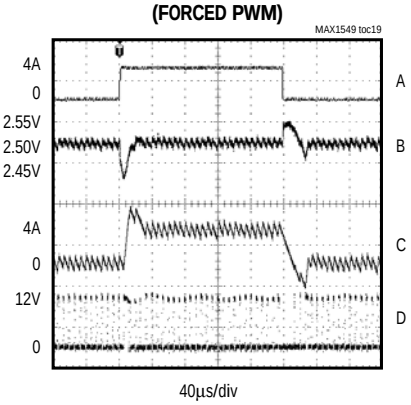
A: LX1, 10V/div
B: 1.0V OUTPUT, 50mV/div
C: LX2, 10V/div
D: 2.5V OUTPUT, 50mV/div

Dual, Interleaved, Fixed-Frequency Step-Down Controller with a Dynamically Adjustable Output

Typical Operating Characteristics (continued)

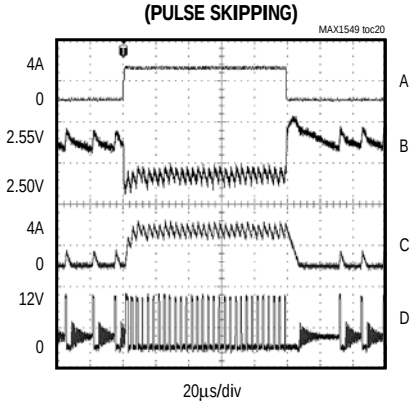
(MAX1549 circuit of Figure 1, V_{IN} = 12V, V_{DD} = V_{CC} = 5V, $\overline{SKIP}$ = GND, FSEL = open, T_A = +25°C, unless otherwise noted.)

2.5V OUTPUT LOAD TRANSIENT (FORCED PWM)



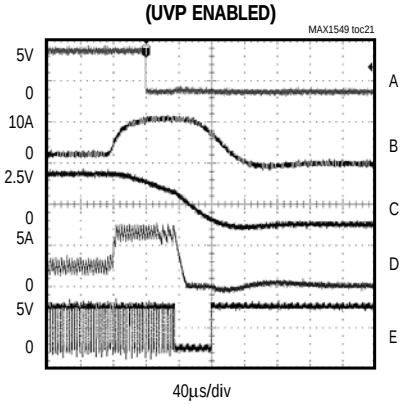
A: I_{OUT2} = 0 TO 4A, 5A/div
B: V_{OUT2} = 2.5V, 100mV/div
$\overline{SKIP}$ = V_{CC}
C: INDUCTOR CURRENT, 5A/div
D: LX2, 10V/div

2.5V OUTPUT LOAD TRANSIENT (PULSE SKIPPING)



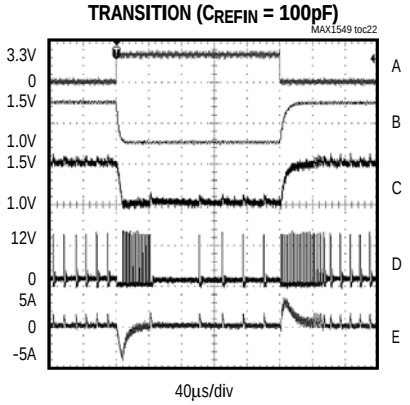
A: I_{OUT2} = 0.2A TO 4A, 5A/div
B: V_{OUT2} = 2.5V, 50mV/div
$\overline{SKIP}$ = GND
C: INDUCTOR CURRENT, 5A/div
D: LX2, 10V/div

OUTPUT OVERLOAD (UVP ENABLED)



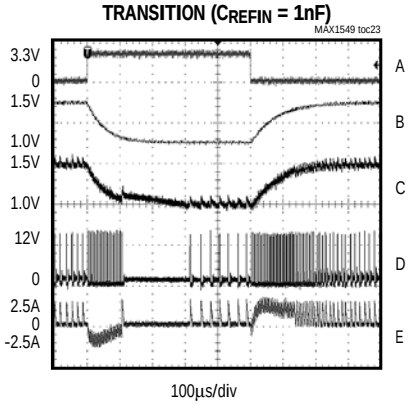
A: PGOOD2, 5V/div
B: LOAD (2.5A TO 10A), 10A/div
C: 2.5V OUTPUT, 2V/div
D: INDUCTOR CURRENT, 5A/div
E: DL2, 5V/div

MAX1549 DYNAMIC OUTPUT VOLTAGE TRANSITION (C_{REFIN} = 100pF)



A: GATE, 5V/div
B: REFIN1, 0.5V/div
C: OUT1 (1.0V TO 1.5V), 0.5V/div
200mA LOAD, $\overline{SKIP}$ = GND
D: LX1, 10V/div
E: INDUCTOR CURRENT, 10A/div

MAX1549 DYNAMIC OUTPUT VOLTAGE TRANSITION (C_{REFIN} = 1nF)



A: GATE, 5V/div
B: REFIN1, 0.5V/div
C: OUT1 (1.0V TO 1.5V), 0.5V/div
200mA LOAD, $\overline{SKIP}$ = GND
D: LX1, 10V/div
E: INDUCTOR CURRENT, 5A/div

Pin Description

PIN	NAME	FUNCTION
1	GND	Analog Ground. Connect backside pad to GND.
2, 20, 25, 31	N.C.	Not Internally Connected
3	REF	2.0V Reference Voltage Output. Bypass to analog ground with a 0.1µF or greater ceramic capacitor. The reference can source up to 100µA for external loads. Loading REF degrades output voltage accuracy according to the REF load-regulation error. The reference shuts down when both MAX1549 outputs are disabled.
4	V_{CC}	Analog Supply Input. Connect to the system supply voltage (+4.5V to +5.5V) through a series 20Ω resistor. Bypass V_{CC} to analog ground with a 1µF or greater ceramic capacitor.
5	CC1	Integrator Capacitor Connection. Connect a 47pF to 1000pF (470pF typ) capacitor from CC1 to analog ground (GND) to set the integration time constant for the main MAX1549 controller (OUT1).
6	ILIM1	Current-Limit Threshold Adjustment for Controller 1. The current-limit threshold defaults to 70mV if ILIM1 is connected to V_{CC}. In adjustable mode, the current-limit threshold across CSH1 and CSL1 is precisely 1/10th the voltage seen at ILIM1 over a 0.5V to 2.0V range. The logic threshold for switchover to the 70mV default value is approximately V_{CC} - 1V.
7	ILIM2	Current-Limit Threshold Adjustment for Controller 2. The current-limit threshold defaults to 70mV if ILIM2 is connected to V_{CC}. In adjustable mode, the current-limit threshold across CSH2 and CSL2 is precisely 1/10th the voltage seen at ILIM2 over a 0.5V to 2.0V range. The logic threshold for switchover to the 70mV default value is approximately V_{CC} - 1V.
8, 9	G0, G1	Buffered N-Channel MOSFET Gate Inputs. See Table 4.
10	FBLANK	Fault-Blanking Select Input. This four-level logic input enables or disables fault blanking and sets the minimum forced-PWM operation time (t_{FBLANK}). When fault blanking is enabled, the MAX1549 blanks the PGOOD1 output and main (OUT1) controller's OVP/UVP fault protection for the selected time period after the controller detects a transition on G0 or G1. Additionally, the main controller enters forced-PWM mode for the duration of t_{FBLANK} anytime G0 or G1 changes states. OUT1 fault protection and PGOOD1 blanking: V_{CC} = 150µs, open = 100µs, REF = 50µs, GND = blanking disabled Automatic forced-PWM transition operation (OUT1 only): V_{CC} = 150µs, open = 100µs, REF = 50µs, GND = 100µs
11	FSEL	Frequency-Select Input. This four-level logic input sets the controller's switching frequency. Connect to GND, REF, V_{CC}, or leave FSEL unconnected (open) to select the following typical switching frequencies: V_{CC} = 400kHz, open = 300kHz, REF = 200kHz, GND = 100kHz
12	ON1	OUT1 Enable Input. Pull to GND to shut down controller 1 (OUT1). Connect to V_{CC} for normal operation. The output is discharged through a 12Ω resistor between OUT1 and GND, and DL1 is forced high after V_{OUT1} drops below 0.3V. A rising edge on ON1 or ON2 clears the fault-protection latch.
13	ON2	OUT2 Enable Input. Pull to GND to shut down controller 2 (OUT2). Connect to V_{CC} for normal operation. The output is discharged through a 12Ω resistor between OUT2 and GND, and DL2 is forced high after V_{OUT2} drops below 0.3V. A rising edge on ON1 or ON2 clears the fault-protection latch.
14	CSH2	Positive Current-Sense Input for Controller 2. Connect to the positive terminal of the current-sense element. Figure 8 describes current-sensing options. The PWM controller does not begin a cycle unless the current sensed is less than the current-limit threshold programmed at ILIM2.

Pin Description (continued)

PIN	NAME	FUNCTION
15	CSL2	Negative Current-Sense Input for Controller 2. Connect to the negative terminal of the current-sense element. Figure 8 describes current-sensing options. The PWM controller does not begin a cycle unless the current sensed is less than the current-limit threshold programmed at ILIM2.
16	FB2	Dual-Mode Feedback Input for Controller 2. Connect to V_{CC} for a +1.8V fixed output or to analog ground (GND) for a +2.5V fixed output. For an adjustable output (0.5V to 2.7V), connect FB2 to a resistive divider from OUT2. The FB2 regulation level is +0.5V.
17	OUT2	Output Voltage-Sense Connection for Controller 2. Connect directly to the positive terminal of the output capacitors as shown in the *Standard Applications Circuit* (Figure 1). OUT2 senses the output voltage to determine the on-time for the high-side switching MOSFET. OUT2 also serves as the feedback input when using the preset internal output voltages as shown in Figure 5. The output capacitor is discharged through an internal 12Ω resistor connected between OUT2 and ground.
18	PGOOD2	Open-Drain Power-Good Output. PGOOD2 is low when the output voltage is more than 10% (typ) above or below the normal regulation point. PGOOD2 is also low during soft-start and shutdown. After the soft-start circuit has terminated, PGOOD2 is high impedance if the output is in regulation.
19	DH2	High-Side Gate-Driver Output for Controller 2. DH2 swings from LX2 to BST2.
21	LX2	Inductor Connection for Controller 2. Connect to the switched side of the inductor. LX2 serves as the lower supply rail for the DH2 high-side gate driver.
22	BST2	Boost Flying-Capacitor Connection for Controller 2. Connect to an external capacitor and diode as shown in Figure 6. An optional resistor in series with BST2 allows the DH2 pullup current to be adjusted.
23	PGND	Power Ground
24	DL2	Low-Side Gate-Driver Output for Controller 2. DL2 swings from PGND to V_{DD}.
26	V_{DD}	Supply Voltage Input for the DL_ Gate Driver. Connect to the system supply voltage (+4.5V to +5.5V). Bypass V_{DD} to power ground with a 1µF or greater ceramic capacitor.
27	DL1	Low-Side Gate-Driver Output for Controller 1. DL1 swings from PGND to V_{DD}.
28	$\overline{SKIP}$	Pulse-Skipping Control Input. This CMOS logic-level input enables or disables the light-load pulse-skipping operation of both outputs. Connect $\overline{SKIP}$ as follows: V_{CC} = OUT1 and OUT2 in forced-PWM mode. GND = OUT1 and OUT2 in pulse-skipping mode.
29	BST1	Boost Flying-Capacitor Connection for Controller 1. Connect to an external capacitor and diode as shown in Figure 6. An optional resistor in series with BST1 allows the DH1 pullup current to be adjusted.
30	LX1	Inductor Connection for Controller 1. Connect to the switched side of the inductor. LX1 serves as the lower supply rail for the DH1 high-side gate driver.
32	DH1	High-Side Gate-Driver Output for Controller 1. DH1 swings from LX1 to BST1.

Pin Description (continued)

PIN	NAME	FUNCTION
33	PGOOD1	Open-Drain Power-Good Output. PGOOD1 is low when the output voltage is more than 10% (typ) above or below the normal regulation point. PGOOD1 is also low during soft-start and shutdown. After the soft-start circuit has terminated, PGOOD1 becomes high impedance if the output is in regulation. For the MAX1549, PGOOD1 is blanked—forced high-impedance state—when FBLANK is enabled and the controller detects a transition on GATE.
34	OUT1	Output-Voltage Sense Connection for Controller 1. Connect directly to the positive terminal of the output capacitors as shown in the *Standard Applications Circuit* (Figure 1). OUT1 senses the output voltage to determine the on-time for the high-side switching MOSFET, and also serves as the feedback input. The output capacitor is discharged through an internal 12Ω resistor connected between OUT1 and ground.
35	CSL1	Negative Current-Sense Input for Controller 1. Connect to the negative terminal of the current-sense element. Figure 8 describes current-sensing options. The PWM controller does not begin a cycle unless the current sensed is less than the current-limit threshold programmed at ILIM1.
36	CSH1	Positive Current-Sense Input for Controller 1. Connect to the positive terminal of the current-sense element. Figure 8 describes current-sensing options. The PWM controller does not begin a cycle unless the current sensed is less than the current-limit threshold programmed at ILIM1.
37, 38, 39	OD1, OD2, OD3	Open-Drain Output. Controlled by G0 and G1 as described in Table 4.
40	REFIN	External Reference Input. REFIN sets the main output voltage ($V_{OUT1} = V_{REFIN}$) of the MAX1549.

Table 1. Component Selection for Standard Applications

COMPONENT	PWM1			PWM2
Input Voltage (V_{IN})	5V to 16V			5V to 16V
Output Voltage (V_{OUT})	G1	G0	V_{OUT1}	2.50V
	0	0	1.50V	
	0	1	1.30V	
	1	0	1.00V	
	1	1	0.70V	
Load Current	6A			5A
Switching Frequency	300kHz			300kHz
$C_{IN\_}$, Input Capacitor	(2) 10µF, 25V Taiyo Yuden TMK432BJ106KM			
$C_{OUT\_}$, Output Capacitor	470µF, 4V, 10mΩ Sanyo POSCAP 4TPD470M			330µF, 6.3V, 10mΩ Sanyo POSCAP 6TPD330M
$N_{H\_}$ High-Side MOSFET	Siliconix Si4800BDY or Fairchild Semiconductor FDS6612A			Siliconix Si4800BDY or Fairchild Semiconductor FDS6612A
$N_{L\_}$ Low-Side MOSFET	Siliconix Si4736DY or Fairchild Semiconductor FDS6670A			Siliconix Si4736DY or Fairchild Semiconductor FDS6670A
$D_{L\_}$ Schottky Rectifier (if needed)	1A, 30V, 0.45V_f Nihon EP10QS03L			1A, 30V, 0.45V_f Nihon EP10QS03L
L_ Inductor	2.5µH Sumida CDRH104-2R5NC			4.7µH Sumida CDRH124-4R7MC
$R_{CS\_}$	12mΩ ±1%, 0.5W resistor IRC LR2010-01-R012F or Dale WSL-2010-R012F			15mΩ ±1%, 0.5W resistor IRC LR2010-01-R015F or Dale WSL-2010-R015F

Table 2. Component Suppliers

SUPPLIER	PHONE	WEBSITE
AVX	843-448-9411 (USA)	www.avx.com
BI Technologies	714-447-2345 (USA)	www.bitechnologies.com
Central Semiconductor	631-435-1110 (USA)	www.centralsemi.com
Coilcraft	800-322-2645 (USA)	www.coilcraft.com
Coiltronics	561-752-5000 (USA)	www.coiltronics.com
Fairchild Semiconductor	888-522-5372 (USA)	www.fairchildsemi.com
International Rectifier	310-322-3331 (USA)	www.irf.com
Kemet	408-986-0424 (USA)	www.kemet.com
Panasonic	800-344-2112 (USA)	www.panasonic.com/industrial
Sanyo	81-72-870-6310 (Japan) 408-749-9714 (USA)	www.secc.co.jp
Siliconix (Vishay)	203-268-6261 (USA)	www.vishay.com
Sumida	81-3-3667-3301 (Japan) 847-545-6700 (USA)	www.sumida.com
Taiyo Yuden	81-3-3833-5441 (Japan) 800-348-2496 (USA)	www.t-yuden.com
TDK	81-3-5201-7241 (Japan) 847-803-6100 (USA)	www.component.tdk.com
TOKO	81-3-3727-1161 (Japan) 847-297-0070 (USA)	www.tokoam.com

Dual, Interleaved, Fixed-Frequency Step-Down Controller with a Dynamically Adjustable Output

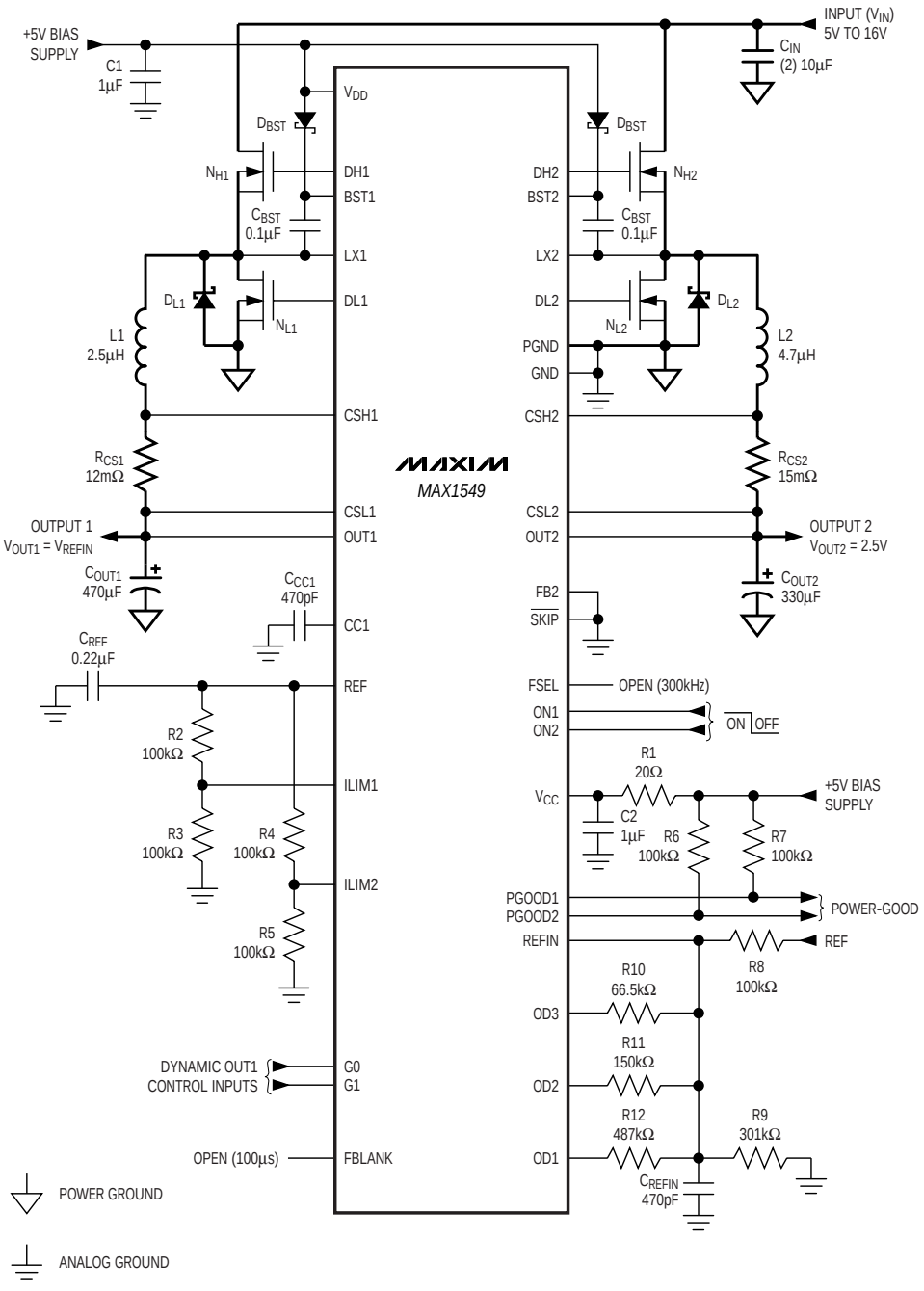


Figure 1. Standard Applications Circuit

Detailed Description

The MAX1549 dual fixed-frequency step-down controller designed for low-voltage power supplies is ideal for graphic processor units (GPUs). The *Standard Applications Circuit* (Figure 1) generates the dynamically adjustable output voltage (OUT1) typically required by graphics processor cores, and a fixed 2.5V output (OUT2) for the local memory used by the GPU. The MAX1549 main output supports up to four output voltages that can be dynamically selected for supporting multiple GPU frequency and sleep states. The interleaved, fixed-frequency architecture provides 180° out-of-phase operation to reduce the input capacitance required to meet the RMS input-current ratings.

Each controller consists of a multi-input PWM comparator, high-side and low-side gate drivers, fault protection, power-good detection, adjustable current-limit circuitry, soft-start, and shutdown logic. The main PWM controller (OUT1) also includes a dedicated reference input; logic-selected, open-drain outputs for dynamically adjusting the output voltage; and an integrator output for improved output-voltage accuracy. The second PWM controller (OUT2) includes a dual-mode feedback network and a multiplexer for preset 2.5V (FB2 = GND), 1.8V (FB2 = V_{CC}), or adjustable output-voltage operation.

See Table 1 for the standard applications circuit's component selection and Table 2 for component manufacturer contact information.

+5V Bias Supply (V_{CC} and V_{DD})

The MAX1549 requires an external 5V bias supply in addition to the battery. Typically, this 5V bias supply is the notebook's 95% efficient, 5V system supply. Keeping the bias supply external to the IC improves efficiency and eliminates the cost associated with the 5V linear regulator that would otherwise be needed to supply the PWM circuit and gate drivers. If stand-alone capability is needed, generate the 5V bias supply with an external linear regulator (V_{IN} > 5.5V) or regulated charge pump (V_{IN} < 4.5V).

The 5V bias supply must provide V_{CC} (PWM controller) and V_{DD} (gate-drive power), so the maximum current drawn is:

$$I_{BIAS} = I_{CC} + f_{SW} (Q_{G(LOW)} + Q_{G(HIGH)})$$
$$= 5mA \text{ to } 50mA \text{ (typ)}$$

where I_{CC} is 1mA (typ), f_{SW} is the switching frequency, and $Q_{G(LOW)}$ and $Q_{G(HIGH)}$ are the MOSFET data sheet's total gate-charge specification limits at V_{GS} = 5V.

The battery input (V_{IN}) and 5V bias inputs (V_{CC} and V_{DD}) can be connected together if the input source is a fixed 4.5V to 5.5V supply. If the 5V bias supply powers up prior to the battery supply, the enable signals (ON1 and ON2 going from low to high) must be delayed until the battery voltage is present to ensure startup.

Fixed-Frequency, Current-Mode PWM Controller

The heart of each current-mode PWM controller is a multi-input, open-loop comparator that sums two signals: the output-voltage error signal with respect to the reference voltage and the slope-compensation ramp (Figure 3). The MAX1549 uses a direct-summing configuration, approaching ideal cycle-to-cycle control over the output voltage without a traditional error amplifier and the phase shift associated with it. The MAX1549 uses a relatively low loop gain, allowing the use of low-cost output capacitors. The low loop gain results in the 0.1% (typ) load-regulation error and helps reduce the output-capacitor size and cost by shifting the unity-gain crossover frequency to a lower level.

Integrator Amplifier (OUT1 Only)

A feedback amplifier forces the DC average of the feedback voltage to equal the reference threshold voltage. This transconductance amplifier integrates the feedback voltage and provides a fine adjustment to the regulation voltage (Figure 2), allowing accurate DC output voltage regulation regardless of the output voltage ripple. The feedback amplifier has the ability to shift the output voltage by ±8%. The differential input voltage range is at least ±80mV total, including DC offset and AC ripple. Use a capacitor value of 47pF to 1000pF (470pF typ).

Dual, Interleaved, Fixed-Frequency Step-Down Controller with a Dynamically Adjustable Output

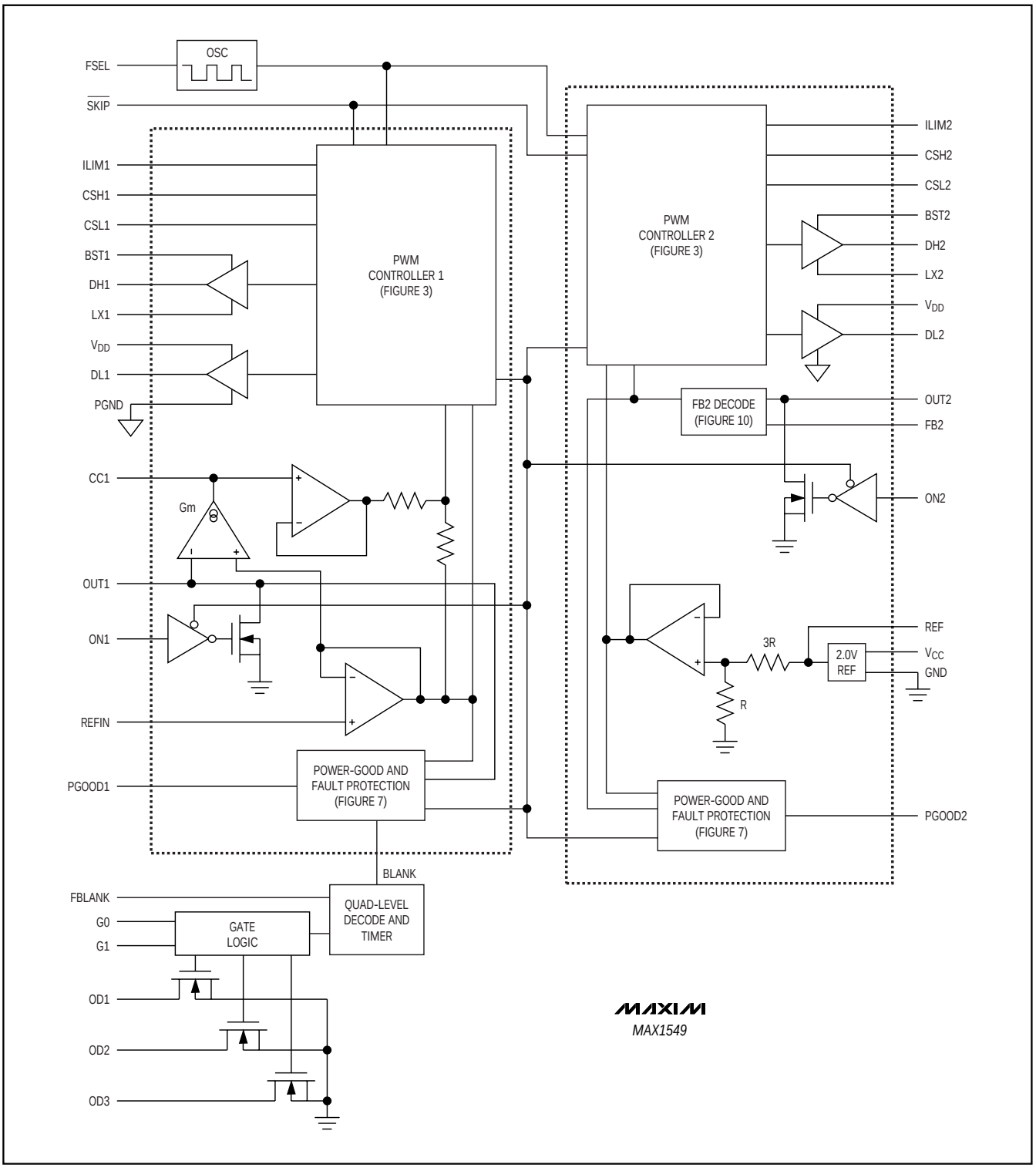


Figure 2. PWM-Controller Detailed Functional Diagram

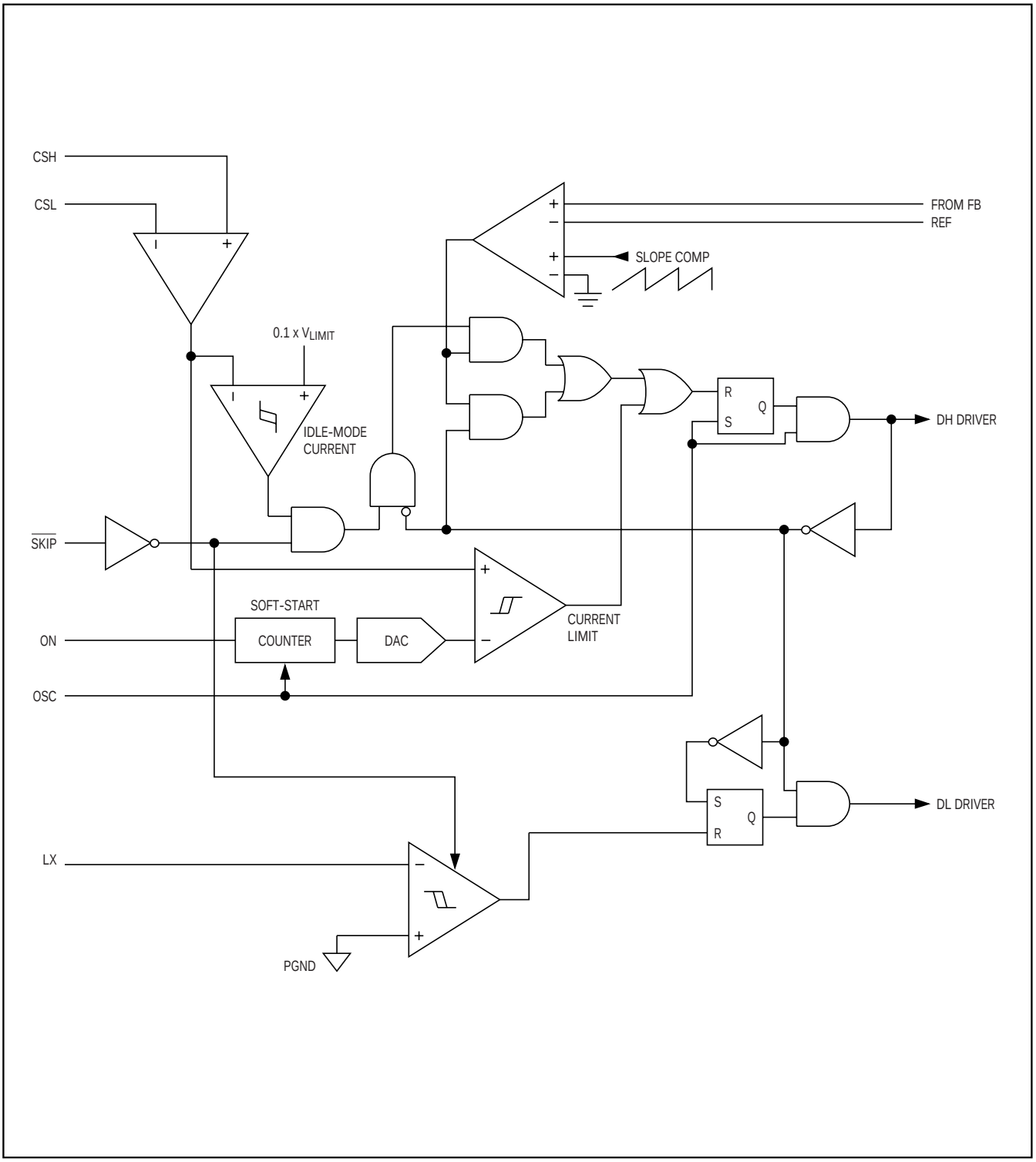


Figure 3. PWM-Comparator Functional Diagram

Table 3. FSEL Configuration

FSEL	SWITCHING FREQUENCY (kHz)
V_{CC}	400
Open	300
REF	200
GND	100

Frequency Selection (FSEL)

The FSEL input selects the PWM-mode switching frequency as shown in Table 3. High-frequency (400kHz) operation optimizes the application for the smallest component size, trading off efficiency due to higher switching losses. This may be acceptable in ultra-portable devices where the load currents are lower. Low-frequency (100kHz) operation offers the best overall efficiency at the expense of component size and board space.

Forced-PWM Mode

The low-noise forced-PWM mode disables the zero-crossing comparator, which controls the low-side switch on-time. This forces the low-side gate-drive waveform to be constantly the complement of the high-side gate-drive waveform, so the inductor current reverses at light loads while DH_ maintains a duty factor of $V_{OUT\_} / V_{IN}$. The benefit of forced-PWM mode is keeping the switching frequency fairly constant. However, forced-PWM operation comes at a cost: the no-load 5V bias current remains between 5mA and 50mA, depending on the external MOSFETs and switching frequency. This additional supply current reduces the light-load efficiency.

In particular, forced-PWM mode avoids audio-frequency noise under light-load conditions, improves the load-transient response, and provides sink-current capability for dynamic output-voltage adjustments. The main MAX1549 controller (OUT1) uses forced-PWM operation during all dynamic output-voltage transitions (G0 or G1 transition detected) to ensure fast, accurate transitions. Since forced-PWM operation disables the zero-crossing comparator, the inductor current reverses under light loads, quickly discharging the output capacitors. FBLANK determines how long the main MAX1549 controller maintains forced-PWM operation—150µs (FBLANK = V_{CC}), 100µs (FBLANK = open or GND), or 50µs (FBLANK = REF).

*Light-Load Operation Control (**SKIP**)*

The MAX1549 includes a light-load operating-mode control input ($\overline{SKIP}$) used to independently enable or disable the zero-crossing comparator for both controllers. When the zero-crossing comparators are enabled ($\overline{SKIP}$ = GND), each controller forces DL_ low when its current-sense inputs detect zero inductor current. This keeps the inductor from discharging the output capacitors and forces the controller to skip pulses under light-load conditions to avoid overcharging the output. When the zero-crossing comparators are disabled ($\overline{SKIP}$ = V_{CC}), each controller maintains PWM operation under light-load conditions (forced-PWM).

The on-time of the step-down controller terminates when the output voltage exceeds the feedback threshold and when the current-sense voltage exceeds the idle-mode current-sense threshold. Under heavy-load conditions, the continuous inductor current remains above the idle-mode current-sense threshold, so the on-time depends only on the feedback-voltage threshold. Under light-load conditions, the controller remains above the feedback-voltage threshold, so the on-time duration depends solely on the idle-mode current-sense threshold, which is approximately 20% of the full-load current-limit threshold set by ILIM_.

When transitioning from pulse-skipping mode to forced-PWM mode ($\overline{SKIP}$ rising edge), DL_ is pulled high immediately if both drivers are low.

Idle-Mode Current-Sense Threshold

The idle-mode current-sense threshold forces a lightly loaded regulator to source a minimum amount of power with each on-time. Since the zero-crossing comparator prevents the switching regulator from sinking current, the controller must skip pulses to avoid overcharging the output. When the clock edge occurs, if the output voltage still exceeds the feedback threshold, the controller does not initiate another on-time. This forces the controller to actually regulate the valley of the output voltage ripple under light-load conditions.

Automatic Pulse-Skipping Crossover

In skip mode, an inherent automatic switchover to PFM takes place at light loads (Figure 4). This switchover is affected by a comparator that truncates the low-side switch on-time at the inductor current's zero crossing. The zero-crossing comparator differentially senses the inductor current across the low-side MOSFET (LX_ to PGND). Once $V_{PGND} - V_{LX\_}$ drops below the 3mV zero-crossing current limit, the comparator forces DL_ low (Figure 3).

This mechanism causes the threshold between pulse-skipping PFM and nonskipping PWM operation to coincide with the boundary between continuous and discontinuous inductor-current operation (also known as the "critical conduction" point). The load-current level at which the PFM/PWM crossover occurs, $I_{LOAD(SKIP)}$, is equal to 1/2 the idle-mode inductor current:

$$I_{LOAD(SKIP)} = \frac{1}{2}\left(\frac{V_{IDLE}}{R_{SENSE}}\right)$$

where V_{IDLE} is the idle-mode threshold (V_{IDLE} = 0.2 x V_{LIMIT} where V_{LIMIT} = 0.1 x V_{ILIM}; see the *Setting the Current Limit* section). The switching waveforms may appear noisy and asynchronous when light loading causes pulse-skipping operation, but this is a normal operating condition that results in high light-load efficiency. Tradeoffs in PFM noise vs. light-load efficiency are made by varying the inductor value. Generally, low inductor values produce a broader efficiency vs. load curve, while higher values result in higher full-load efficiency (assuming the coil resistance remains fixed) and less output voltage ripple. Penalties for using higher inductor values include larger size and degraded load-transient response (especially at low input-voltage levels).

Output Voltage

DC-output accuracy specifications in the *Electrical Characteristics* table refer to the error-comparator threshold. When the inductor continuously conducts (PWM operation), the MAX1549 regulates the peak of the output ripple, so the actual DC output voltage depends on the error-comparator threshold, the slope-compensation amplitude, and the output voltage ripple. For PWM operation (continuous conduction), the output voltage is defined by the following equation:

$$V_{OUT\_(PWM)} = V_{NOM}\left(1 - \frac{A_{SLOPE}\ V_{NOM}}{V_{IN}}\right) - \left(\frac{V_{RIPPLE}}{2}\right)$$

where V_{NOM} is the nominal output voltage, A_{SLOPE} equals 1%, and V_{RIPPLE} is the output voltage ripple (typically V_{RIPPLE} = ESR x $\Delta I_{INDUCTOR}$ as described in the *Output Capacitor Selection* section).

In discontinuous conduction ($I_{OUT} < I_{LOAD(SKIP)}$), the MAX1549 regulates the valley of the output ripple, and the output voltage has a DC regulation level higher than the error-comparator threshold by approximately 1.5% due to the slope compensation.

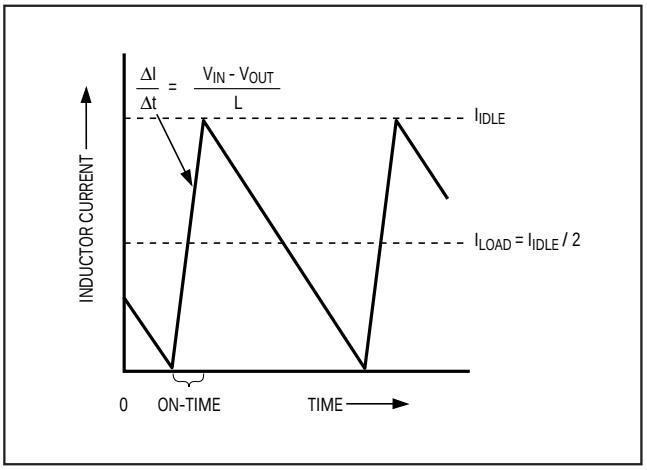


Figure 4. Pulse-Skipping/Discontinuous Crossover Point

For PFM operation (discontinuous conduction), the output voltage is defined by the following equation:

$$V_{OUT(PFM)} = V_{NOM} + \frac{1}{2}\left(\frac{f_{SW}}{f_{OSC}}\right) I_{IDLE} \times ESR$$

where f_{OSC} is the maximum switching frequency set by FSEL, f_{SW} is the actual switching frequency, and I_{IDLE} is the idle-mode inductor current when pulse skipping.

Dynamic Output Voltages (OUT1 Only)

The MAX1549 regulates OUT1 to the voltage set at REFIN. By changing the voltage at REFIN, the MAX1549 can be used in applications that require dynamic output-voltage changes between two set points. Figure 1 shows a dynamically adjustable resistive voltage-divider network at REFIN. Using the G0 and G1 gate inputs and the open-drain outputs (OD1, OD2, and OD3), resistors can be switched in and out of the REFIN resistor-divider, dynamically changing the voltage at REFIN. The open-drain outputs are activated by the G0 and G1 gate inputs as shown in Table 4. The main output voltage is determined by the following equation:

$$V_{OUT1} = V_{REF}\left(\frac{R_{EQ}}{R8 + R_{EQ}}\right)$$

where R_{EQ} is the equivalent resistance between REFIN and ground (see Figure 1 and Table 4).

The main MAX1549 controller (OUT1) automatically enters forced-PWM operation after detecting a G0 or G1 transition (rising or falling edge), and remains in forced-PWM mode for a minimum time selected by FBLANK (Table 5).

Table 4. Open-Drain Output States

INPUTS		OUTPUTS			R_{EQ}
G1	G0	OD1	OD2	OD3	
0	0	High-Z	High-Z	High-Z	R9
0	1	0	High-Z	High-Z	R9 // R12
1	0	High-Z	0	High-Z	R9 // R11
1	1	High-Z	High-Z	0	R9 // R10

Forced-PWM operation is required to ensure fast, accurate negative voltage transitions when REFIN is lowered. Since forced-PWM operation disables the zero-crossing comparator, the inductor current can reverse under light loads, quickly discharging the output capacitors. If fault blanking is enabled, the MAX1549 disables the main controller's (OUT1) output fault protection (OVP and UVP), and forces PGOOD1 to a high-impedance state for the period selected by FBLANK (Table 5).

For a step voltage change at REFIN, the rate-of-change of the output voltage is limited by the inductor current ramp, the total output capacitance, the current limit, and the load during the transition. The inductor current ramp is limited by the voltage across the inductor and the inductance. The total output capacitance determines how much current is needed to change the output voltage. Additional load current slows down the output-voltage change during a positive REFIN voltage change, and speeds up the output-voltage change during a negative REFIN voltage change. Increasing the current-limit setting speeds up a positive output-voltage change.

Adding a capacitor across REFIN and GND filters noise and controls the rate-of-change of the REFIN voltage during dynamic transitions. With the additional capacitance, the REFIN voltage slews between the two set points with a time constant given by $R_{REFIN} \times C_{REFIN}$, where R_{REFIN} is the equivalent parallel resistance seen by the slew capacitor during the transition:

$$\tau_{REFIN} = \left(\frac{R8 \times R_{EQ}}{R8 + R_{EQ}}\right) C_{REFIN}$$

Dual-Mode Feedback (OUT2 Only)

The MAX1549's dual-mode operation allows the selection of common voltages without requiring external components (Figure 5). For the secondary controller (OUT2), connect FB2 to GND for a fixed 2.5V output, to V_{CC} for a fixed 1.8V output, or connect FB2 directly to OUT2 for a fixed 0.5V output. The main controller (OUT1) of the MAX1549 regulates to the voltage set at REFIN ($V_{FB1} = V_{REFIN}$) and does not support dual-mode operation.

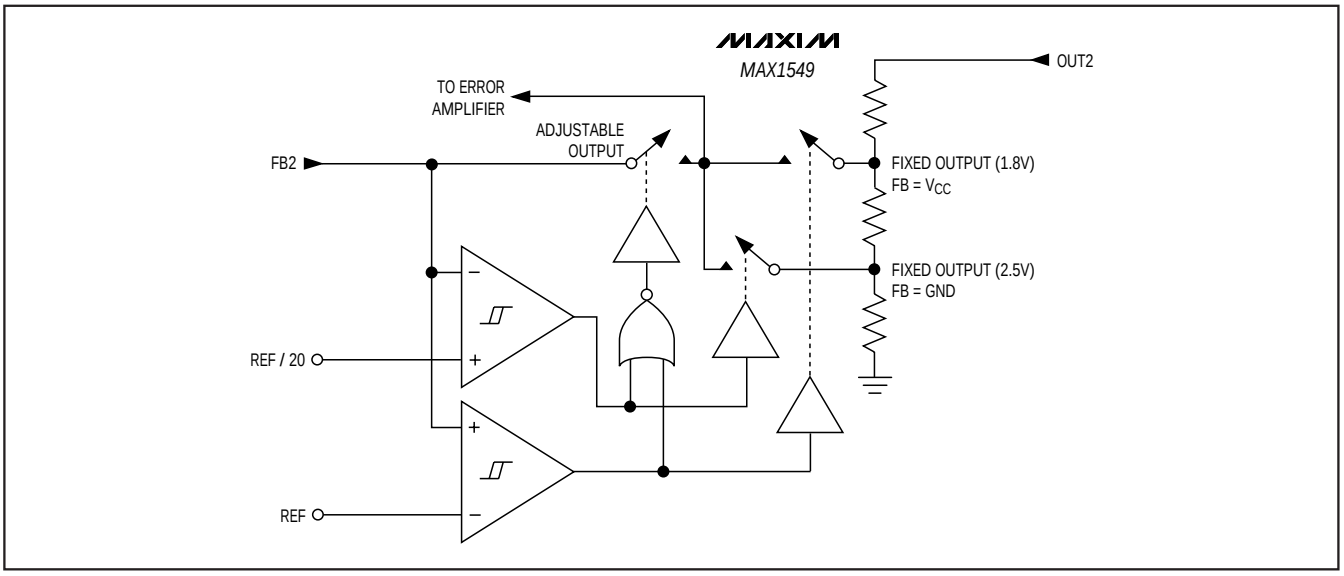


Figure 5. Second Controller's Dual-Mode Feedback

Alternately, the secondary output voltage (OUT2) can be adjusted from 0.5V to 2.7V using a resistive voltage-divider. The MAX1549 regulates FB2 to a fixed 0.5V reference voltage, so the secondary output voltage can be determined with the following equation:

$$V_{OUT2} = V_{FB2}\left(1 + \frac{R_A}{R_B}\right)$$

where V_{FB2} = 0.5V, R_A is the resistor from the output to FB2, and R_B is the resistor from FB2 to analog ground.

Current-Limit Protection (ILIM_)

The current-limit circuit uses differential current-sense inputs (CSH_ and CSL_) to limit the peak inductor current. If the magnitude of the current-sense signal exceeds the current-limit threshold, the PWM controller turns off the high-side MOSFET (Figure 3). At the next rising edge of the internal oscillator, the PWM controller does not initiate a new cycle unless the current-sense signal drops below the peak current-limit threshold. The actual maximum load current is less than the peak current-limit threshold by an amount equal to 1/2 the inductor ripple current. Therefore, the maximum load capability is a function of the current-limit threshold, current-sense resistance, inductor value, switching frequency, and duty cycle (V_{OUT} / V_{IN}).

Connect ILIM_ to V_{CC} for the 70mV default threshold, or adjust the current-limit threshold with an external resistor-divider at ILIM_. Use a 2µA to 20µA divider current for accuracy and noise immunity. The current-limit threshold adjustment range is from 50mV to 200mV. In the adjustable mode, the current-limit threshold voltage equals precisely 1/10th the voltage seen at ILIM_ (V_{LIMIT} = $0.1V_{ILIM\_}$). The logic threshold for switchover to the 70mV default value is approximately V_{CC} - 1V.

Carefully observe the PC board layout guidelines to ensure noise and DC errors do not corrupt the differential current-sense signals seen by CSH_ and CSL_. Place the IC close to the sense resistor with short, direct traces, making a Kelvin-sense connection to the current-sense resistor.

MOSFET Gate Drivers (DH_, DL_)

The DH_ and DL_ drivers are optimized for driving moderately sized, high-side and larger, low-side power MOSFETs. This is consistent with the low duty factor seen in notebook applications, where a large V_{IN} - V_{OUT} differential exists. An adaptive dead-time circuit monitors the DL_ output and prevents the high-side MOSFET from turning on until DL_ is fully off. A similar adaptive dead-time circuit monitors the DH_ output to prevent the low-side MOSFET from turning on until DH_ is fully off. There must be a low-resistance, low-inductance path from the DL_ and DH_ drivers to the MOSFET gates for the adaptive dead-time circuits to work properly. Otherwise, the MAX1549 interprets the MOSFET gates as “off” while charge actually remains on the gate. Use very short, wide traces (50 mils to 100 mils wide if the MOSFET is 1in from the driver).

The internal pulldown transistor that drives DL_ low is robust, with a 0.5Ω (typ) on-resistance. This helps prevent DL_ from being pulled up due to capacitive coupling from the drain to the gate of the low-side MOSFETs when the inductor node (LX_) quickly switches from ground to V_{IN}. Applications with high input voltages and long, inductive driver traces may require additional gate-to-source capacitance to ensure fast-rising LX_ edges do not pull up the low-side MOSFETs’ gate voltage, causing shoot-through currents. The capacitive coupling between LX_ and DL_ created by the MOSFETs’ gate-to-drain capacitance (C_{RSS}), gate-to-source capacitance (C_{ISS} - C_{RSS}), and additional board parasitics should not exceed the following minimum threshold:

$$V_{GS(TH)} > V_{IN}\left(\frac{C_{RSS}}{C_{ISS}}\right)$$

Lot-to-lot variation of the threshold voltage can cause problems in marginal designs. Typically, adding a 4700pF between DL_ and power ground (C_{NL} in Figure 6), close to the low-side MOSFETs, greatly reduces the voltage coupling. Do not exceed 22nF of total gate capacitance to prevent excessive turn-off delays.

Alternately, shoot-through currents can be caused by a combination of fast high-side MOSFETs and slow low-side MOSFETs. If the turn-off delay time of the low-side MOSFET is too long, the high-side MOSFETs turn on before the low-side MOSFETs have actually turned off. Adding a resistor less than 10Ω in series with BST_ slows down the high-side MOSFET turn-on time, eliminating the shoot-through currents without degrading the turn-off time (Figure 6). Slowing down the high-side MOSFET also reduces the LX_ node rise time, thereby reducing the EMI and high-frequency coupling responsible for switching noise.

Power-Up Sequence

Power-on reset (POR) occurs when V_{CC} rises above approximately 2V, resetting the fault latch and soft-start counter, powering up the reference, and preparing the PWM controllers for operation. Until V_{CC} reaches 4.25V (typ), the V_{CC} undervoltage-lockout (UVLO) circuitry inhibits switching. The controller inhibits switching by pulling DH_ low and forcing DL_ high. When V_{CC} rises above 4.25V and ON_ is driven high, the activated controller initializes soft-start and starts switching.

Dual, Interleaved, Fixed-Frequency Step-Down Controller with a Dynamically Adjustable Output

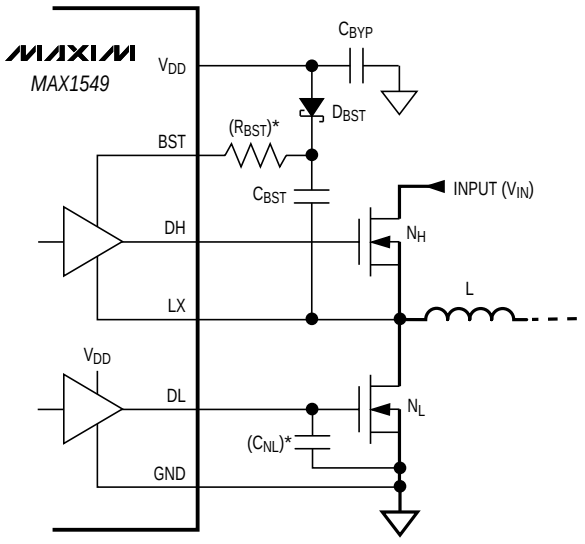


Figure 6. Optional Gate-Driver Circuitry

Digital Soft-Start

Soft-start allows a gradual increase of the internal current-limit level during startup to reduce the input surge currents. Both controllers contain an internal digital soft-start circuit. In shutdown mode or input UVLO, the controller resets the soft-start counter to zero.

The MAX1549 divides the soft-start period into five phases. During the first phase, the controller limits the peak current limit to only 20% of the full current limit. If the output does not reach regulation within 128 clock cycles (1 / f_{OSC}), soft-start enters the second phase and increments the current limit by another 20%. This process repeats until soft-start reaches the maximum current limit after 512 clock cycles or until the output reaches the nominal regulation voltage, whichever occurs first (see the Soft-Start Waveforms in the *Typical Operating Characteristics*). The exact rise time of the output voltage depends on the output capacitance and load current.

Soft-Shutdown

Soft-shutdown slowly discharges the output capacitance, providing a damped shutdown response. This eliminates the slightly negative output voltages caused by quickly discharging the output through the inductor and low-side MOSFET. Both controllers contain separate soft-shutdown circuits.

When the controller is disabled—ON_ pulled low, the UV fault latch set, or input UVLO triggered—the MAX1549 discharges the respective output through an internal 12Ω switch to ground. While the output discharges, the MAX1549 forces DL_ low and disables the PWM controller, but the reference remains active to provide an accurate threshold. Once the output voltage drops below 0.3V, the MAX1549 pulls DL_ high, effectively clamping the output and LX_ switching node to ground. The reference shuts down once both outputs are disabled and discharged below 0.3V.

Power-Good Output (PGOOD_)

The MAX1549 includes separate open-drain outputs for the power-good window comparators (Figure 7) that monitor each output continuously (except during main-output fault blanking; see the *Fault and Power-Good Blanking* section). The controller actively holds PGOOD_ low in shutdown and during soft-start. Once the digital soft-start terminates, PGOOD_ becomes high impedance as long as the respective output voltage is within ±10% of the nominal regulation voltage. When either output voltage drops 10% below or rises 10% above the nominal regulation voltage, the MAX1549 pulls the respective PGOOD_ output low. Any fault condition forces both PGOOD1 and PGOOD2 low until the fault latch is cleared by toggling ON1 or ON2, or cycling V_{CC} power below 1V. For logic-level output voltages, connect an external pullup resistor between PGOOD_ and V_{CC}. A 100kΩ resistor works well in most applications.

The power-good window comparators are completely independent of the overvoltage and undervoltage-protection fault comparators.

Fault Protection

Overvoltage Protection (OVP)

If either output voltage rises above 114.5% of its nominal regulation voltage, the OVP circuit sets the fault latch, pulls PGOOD1 and PGOOD2 low, shuts down both PWM controllers, and immediately pulls DH_ low and forces DL_ high. This turns on the synchronous-rectifier MOSFETs with 100% duty, rapidly discharging the output capacitors and clamping both outputs to ground. However, immediately latching DL_ high typically causes slightly negative output voltages due to

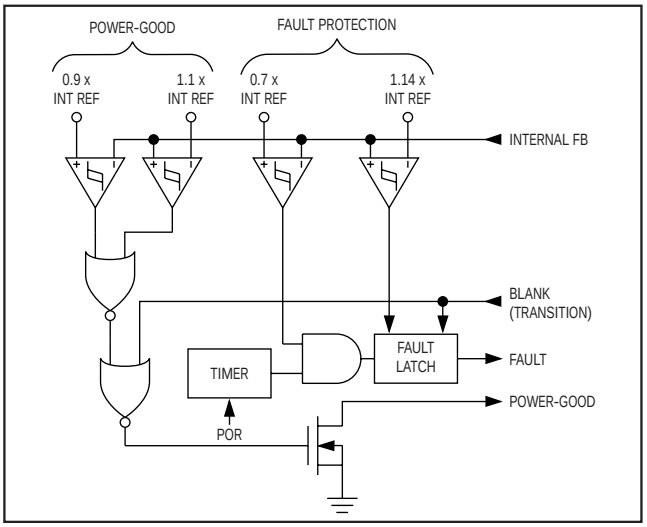


Figure 7. Power-Good and Fault Protection

the energy stored in the output LC at the instant the OV fault occurs. If the load cannot tolerate a negative voltage, place a power Schottky diode across the output to act as a reverse-polarity clamp. If the condition that caused the overvoltage persists (such as a shorted high-side MOSFET), the battery fuse blows. The main controller temporarily blanks OVP after transitions are detected on G0 or G1 (FBLANK enabled). Toggle ON1 or ON2, or cycle V_{CC} power below 1V, to clear the fault latch and restart the controller.

Undervoltage Protection (UVP)

Each controller has an output UVP circuit that activates 4096 clock cycles (1 / f_{OSC}) after the controller is enabled. If either output voltage drops below 70% of its nominal regulation voltage, the MAX1549 sets the fault latch, pulls PGOOD1 and PGOOD2 low, and shuts down both controllers using discharge mode (see the *Soft-Shutdown* section). When each output voltage drops to 0.3V, its synchronous rectifier turns on and clamps the output to GND. The main controller temporarily blanks UVP after transitions are detected on G0 or G1 (FBLANK enabled). Toggle ON1 or ON2, or cycle V_{CC} power below 1V, to clear the fault latch and restart the controller.

Thermal Fault Protection

The MAX1549 features a thermal fault-protection circuit. When the junction temperature rises above +160°C, a thermal sensor activates the fault latch, pulls PGOOD1 and PGOOD2 low, and shuts down both controllers using discharge mode. Toggle ON1 or ON2, or cycle V_{CC} power below 1V, to reactivate the controller after the junction temperature cools by 15°C.

Table 5. FBLANK Configuration Table

FBLANK	OUT1 FAULT AND PGOOD1 BLANKING	OUT1 FORCED-PWM DURATION (TYP) (µs)
V_{CC}	Enabled (150µs)	150
Open	Enabled (100µs)	100
REF	Enabled (50µs)	50
GND	Disabled	100

Fault and Power-Good Blanking (FBLANK)

The main MAX1549 controller (OUT1) automatically enters forced-PWM operation during all dynamic output-voltage transitions (G0 or G1 transition detected) to ensure fast, accurate transitions. FBLANK determines how long the main controller maintains forced-PWM operation (Table 5)—150µs (FBLANK = V_{CC}), 100µs (FBLANK = open or GND), or 50µs (FBLANK = REF).

When fault blanking is enabled (FBLANK = V_{CC}, open, or REF), the MAX1549 also disables the overvoltage and undervoltage fault protection for OUT1, and forces PGOOD1 to a high-impedance state during the transition period selected by FBLANK (Table 5). This prevents fault protection from latching off the MAX1549 and keeps the PGOOD1 signal from going low while the output-voltage transition occurs.

Design Procedure

Firmly establish the input voltage range and maximum load current before choosing a switching frequency and inductor operating point (ripple-current ratio). The primary design tradeoff lies in choosing a good switching frequency and inductor operating point, and the following four factors dictate the rest of the design:

Input Voltage Range: The maximum value ($V_{IN(MAX)}$) must accommodate the worst-case, high AC-adapter voltage. The minimum value ($V_{IN(MIN)}$) must account for the lowest battery voltage minus the voltage drops associated with the connectors, fuses, and battery-selector switches. If there is a choice at all, lower input voltages result in better efficiency. The minimum and maximum input voltage range is restricted by the minimum and maximum duty-cycle limits specified in the *Electrical Characteristics* table:

$$V_{IN(MIN)} > \frac{V_{OUT}}{D_{MAX}} \text{ and } V_{IN(MAX)} < \frac{V_{OUT}}{t_{ON(MIN)} f_{OSC}}$$

where D_{MAX} is the 91% maximum duty-cycle limit, $t_{ON(MIN)}$ is the 200ns minimum off-time, and f_{OSC} is the switching frequency selected by FSEL. Since the maximum input voltage range is restricted by the switching frequency and output voltage, lower frequency operation might be required for high input-to-output voltage applications.

Dual, Interleaved, Fixed-Frequency Step-Down Controller with a Dynamically Adjustable Output

Maximum Load Current: There are two values to consider. The peak inductor current (I_{PEAK}) determines the instantaneous component stresses and filtering requirements and thus drives output capacitor selection, inductor saturation rating, and the design of the current-limit circuit. The maximum continuous load current ($I_{LOAD(MAX)}$) determines the thermal stresses and thus drives the selection of input capacitors, MOSFETs, and other critical heat-contributing components.

Switching Frequency: This choice determines the basic tradeoff between size, efficiency, and maximum input voltage range. The optimum frequency is largely a function of maximum input voltage, due to MOSFET switching losses that are proportional to frequency and V_{IN}^2. The optimum frequency is also a moving target, due to rapid improvements in MOSFET technology that are making higher frequencies more practical.

Inductor Operating Point: This choice provides tradeoffs between size vs. efficiency and transient response vs. output ripple. Low inductor values provide better transient response and smaller size, but also result in lower efficiency and higher output ripple due to increased ripple currents. The minimum practical inductor value is one that causes the circuit to operate at the edge of critical conduction (where the inductor current just touches zero with every cycle at maximum load). Inductor values lower than this grant no further size-reduction benefit. The optimum operating point is usually found between 20% and 50% ripple current. When pulse skipping ($\overline{SKIP}$ low and light loads), the inductor value also determines the load-current value at which PFM/PWM switchover occurs.

Inductor Selection

The switching frequency and inductor operating point determine the inductor value as follows:

$$L = \frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN} \times f_{OSC} \times I_{LOAD(MAX)} \times LIR}$$

For example: $I_{LOAD(MAX)}$ = 5A, V_{IN} = 12V, V_{OUT} = 2.5V, f_{OSC} = 300kHz, 30% ripple current or LIR = 0.3:

$$L = \frac{2.5V \times (12V - 2.5V)}{12V \times 300kHz \times 5A \times 0.3} = 4.40\mu H$$

Find a low-loss inductor with the lowest possible DC resistance that fits in the allotted dimensions. Ferrite cores are often the best choice, although powdered iron is inexpensive and can work well at 200kHz. The core must be large enough not to saturate at the peak inductor current (I_{PEAK}):

$$I_{PEAK} = I_{LOAD(MAX)} \left(1 + \frac{LIR}{2}\right)$$

Most inductor manufacturers provide inductors in standard values, such as 1.0µH, 1.5µH, 2.2µH, 3.3µH, etc. Also look for nonstandard values, which can provide a better compromise in LIR across the input voltage range. If using a swinging inductor (where the no-load inductance decreases linearly with increasing current), evaluate the LIR with properly scaled inductance values.

Transient Response

The inductor ripple current also impacts transient-response performance, especially at low V_{IN} - V_{OUT} differentials. Low inductor values allow the inductor current to slew faster, replenishing charge removed from the output-filter capacitors by a sudden load step. The total output voltage sag is the sum of the voltage sag while the inductor is ramping up and the voltage sag before the next pulse can occur:

$$V_{SAG} = \frac{L(\Delta I_{LOAD(MAX)})^2}{2C_{OUT}(V_{IN} \times D_{MAX} - V_{OUT})}$$

$$+ \frac{\Delta I_{LOAD(MAX)}(T - \Delta T)}{C_{OUT}}$$

where D_{MAX} is the maximum duty factor (see the *Electrical Characteristics* table), T is the cycle period (1 / f_{OSC}), ΔT equals V_{OUT} / V_{IN} x T when in PWM mode, or L x 0.2 x I_{MAX} / (V_{IN} - V_{OUT}) when in skip mode. The amount of overshoot during a full-load to no-load transient due to stored inductor energy can be calculated as:

$$V_{SOAR} \approx \frac{(\Delta I_{LOAD(MAX)})^2 L}{2C_{OUT}V_{OUT}}$$

Setting the Peak Current Limit

The minimum current-limit threshold must be great enough to support the maximum load current when the current limit is at the minimum tolerance value. The peak inductor current occurs at $I_{LOAD(MAX)}$ plus 1/2 the ripple current; therefore:

$$I_{LIMIT} > I_{LOAD(MAX)} + \left(\frac{I_{LOAD(MAX)} LIR}{2} \right)$$

where $I_{LIMIT\_}$ equals the minimum current-limit threshold voltage divided by the current-sense resistance (R_{SENSE}). For the 70mV default setting, the minimum current-limit threshold is 65mV.

Connect ILIM_ to V_{CC} for a default 70mV current-limit threshold. In adjustable mode, the current-limit threshold is precisely 1/10th the voltage seen at ILIM_. For an adjustable threshold, connect a resistive-divider from REF to analog ground (GND) with ILIM_ connected to the center tap. The external 500mV to 2V adjustment range corresponds to a 50mV to 200mV current-limit threshold. When adjusting the current limit, use 1% tolerance resistors and a divider current of approximately 10µA to prevent significant inaccuracy in the current-limit tolerance.

The current-sense method (Figure 8) and magnitude determine the achievable current-limit accuracy and power loss. Typically, higher current-sense limits provide more noise immunity, but also dissipate more power. Most applications employ a current-limit threshold (V_{LIMIT}) of 50mV to 100mV, so the sense resistor can be determined by:

$$R_{SENSE} = \frac{V_{LIMIT}}{I_{LIMIT}}$$

For the best current-sense accuracy and overcurrent protection, use a 1% tolerance current-sense resistor between the inductor and output as shown in Figure 8A. This configuration constantly monitors the inductor current, allowing accurate current-limit protection.

Alternately, high-power applications that do not require highly accurate current-limit protection can reduce the overall power dissipation by connecting a series RC circuit across the inductor (Figure 8B) with an equivalent time constant:

$$\frac{L}{R_{DCR}} = C_{EQL} \times R_{EQL}$$

where R_{DCR} is the inductor's series DC resistance. In this configuration, the current-sense resistance equals

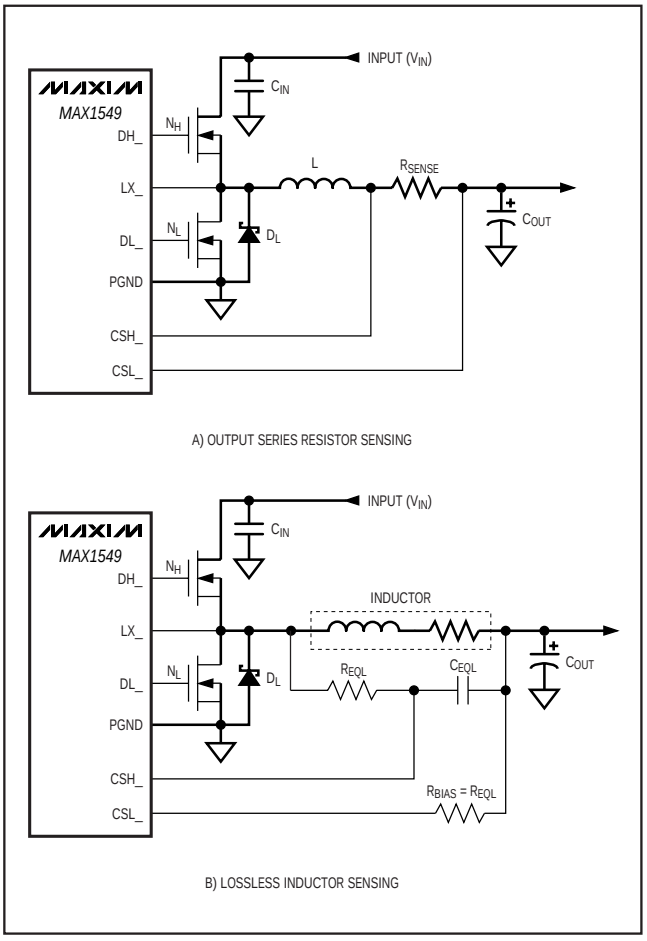


Figure 8. Current-Sense Configurations

the inductor's DC resistance ($R_{SENSE} = R_{DCR}$). Use the worst-case inductance and R_{DCR} values provided by the inductor manufacturer, adding some margin for the inductance drop over temperature and load.

Output Capacitor Selection

The output-filter capacitor must have low enough equivalent series resistance (ESR) to meet output ripple and load-transient requirements, yet have high enough ESR to satisfy stability requirements.

For processor core voltage converters and other applications where the output is subject to severe load transients, the output capacitor's size depends on how much ESR is needed to prevent the output from dipping too low under a load transient. Ignoring the sag due to finite capacitance:

$$R_{ESR} \leq \frac{V_{STEP}}{\Delta I_{LOAD(MAX)}}$$

Dual, Interleaved, Fixed-Frequency Step-Down Controller with a Dynamically Adjustable Output

In applications without large and fast load transients, the output capacitor's size often depends on how much ESR is needed to maintain an acceptable level of output voltage ripple. The output voltage ripple of a step-down controller equals the total inductor ripple current multiplied by the output capacitor's ESR. Therefore, the maximum ESR required to meet the ripple specifications is:

$$R_{ESR} \leq \frac{V_{RIPPLE}}{I_{LOAD(MAX)}LIR}$$

The actual capacitance value required relates to the size needed to achieve low ESR, as well as to the chemistry of the capacitor technology. Thus, the capacitor is usually selected by ESR and voltage rating rather than by capacitance value (this is true of tantalums, OS-CONs, polymers, and other electrolytics).

When using low-capacity filter capacitors, such as ceramic capacitors, size is usually determined by the capacity needed to prevent V_{SAG} and V_{SOAR} from causing problems during load transients. Generally, once enough capacitance is added to meet the overshoot requirement, undershoot at the rising load edge is no longer a problem (see the V_{SAG} and V_{SOAR} equations in the *Transient Response* section). However, low-capacity filter capacitors typically have high ESR zeros that can affect the overall stability (see the *Output-Capacitor Stability Considerations* section).

Output-Capacitor Stability Considerations

The MAX1549 controllers rely on the output voltage ripple, which can be defined as the inductor current ripple times the output capacitor's ESR, to generate the current-mode control signal required for stable operation. Therefore, the controller's stability is determined by the value of the ESR zero relative to the switching frequency. The boundary of instability is given by the following equation:

$$f_{ESR} \leq \frac{f_{OSC}}{\pi}$$

where:

$$f_{ESR} = \frac{1}{2\pi R_{ESR} C_{OUT}}$$

For a typical 300kHz application, the ESR zero frequency must be well below 95kHz, preferably below 50kHz. Tantalum and OS-CON capacitors in widespread use at the time of publication have typical ESR zero frequencies of 25kHz. In the design example used for inductor selection, the ESR needed to support 25mV_{P-P} ripple is 25mV / 1.5A = 16.7mΩ. One 220µF/4V Sanyo polymer (TPE) capacitor provides 15mΩ (max) ESR. This results in a zero at 48kHz, well within the bounds of stability.

Do not put high-value ceramic capacitors directly across the feedback sense point without taking precautions to ensure stability. Large ceramic capacitors can have a high-ESR zero frequency and cause erratic, unstable operation. However, it is easy to add enough series resistance by placing the capacitors a couple inches downstream from the feedback sense point, which should be as close as possible to the inductor.

Unstable operation manifests itself in two related but distinctly different ways: duty-cycle variation and fast-feedback loop instability. Duty-cycle variation occurs due to noise on the output or because the ESR is so low that there is not enough voltage ramp in the output-voltage signal. This "fools" the error comparator into extending the on-time, forcing the next cycle to terminate its on-time early. Duty-cycle variation is more annoying than harmful, resulting in nothing worse than increased output ripple. However, it can indicate the possible presence of loop instability due to insufficient ESR. Loop instability can result in oscillations at the output after line or load steps. Such perturbations are usually damped, but can cause the output voltage to rise above or fall below the tolerance limits.

The easiest method for checking stability is to apply a very fast zero-to-max load transient and carefully observe the output-voltage-ripple envelope for overshoot and ringing. It can help to simultaneously monitor the inductor current with an AC current probe. Do not allow more than one cycle of ringing after the initial step-response under/overshoot.

Input Capacitor Selection

The input capacitor must meet the RMS ripple current requirement (I_{RMS}) imposed by the switching currents. For a single step-down converter, the RMS input ripple current is defined by the output load current (I_{OUT}), input voltage, and output voltage, with the worst-case condition occurring at $V_{IN} = 2V_{OUT}$:

$$I_{RMS} = I_{OUT}\left(\frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}}\right)$$

For a dual 180° interleaved controller, the out-of-phase operation reduces the RMS input ripple current, effectively lowering the input capacitance requirements.

When both outputs operate with a duty cycle less than 50% (V_{IN} > $2V_{OUT}$), the RMS input ripple current is defined by the following equation:

$$I_{RMS} = \sqrt{\left(\frac{V_{OUT1}}{V_{IN}}\right) I_{OUT1}(I_{OUT1} - I_{IN}) + \left(\frac{V_{OUT2}}{V_{IN}}\right) I_{OUT2}(I_{OUT2} - I_{IN})}$$

where I_{IN} is the average input current:

$$I_{IN} = \left(\frac{V_{OUT1}}{V_{IN}}\right) I_{OUT1} + \left(\frac{V_{OUT2}}{V_{IN}}\right) I_{OUT2}$$

For most applications, nontantalum chemistries (ceramic, aluminum, or OS-CON) are preferred due to their resilience to power-up surge currents typical of systems with a mechanical switch or connector in series with the input. If the MAX1549 is operated as the second stage of a two-stage power-conversion system, tantalum input capacitors are acceptable. In either configuration, choose a capacitor that has less than 10°C temperature rise at the RMS input current for optimal reliability and lifetime.

Power MOSFET Selection

Most of the following MOSFET guidelines focus on the challenge of obtaining high load-current capability when using high-voltage (>20V) AC adapters. Low-current applications usually require less attention.

The high-side MOSFET (N_H) must be able to dissipate the resistive losses plus the switching losses at both $V_{IN(MIN)}$ and $V_{IN(MAX)}$. Ideally, the losses at $V_{IN(MIN)}$ should be roughly equal to the losses at $V_{IN(MAX)}$, with lower losses in between. If the losses at $V_{IN(MIN)}$ are significantly higher, consider increasing the size of N_H. Conversely, if the losses at $V_{IN(MAX)}$ are significantly higher, consider reducing the size of N_H. If V_{IN} does not vary over a wide range, maximum efficiency is achieved by selecting a high-side MOSFET (N_H) that has conduction losses equal to the switching losses.

Choose a low-side MOSFET (N_L) that has the lowest possible on-resistance ($R_{DS(ON)}$), comes in a moderate-sized package (i.e., 8-pin SO, DPAK, or D^2PAK), and is reasonably priced. Ensure that the MAX1549 DL_ gate driver can supply sufficient current to support the gate charge and the current injected into the parasitic drain-to-gate capacitor caused by the high-side MOSFET turning on; otherwise, cross-conduction problems can occur. Switching losses are not an issue for the low-side MOSFET since it is a zero-voltage switched device when used in the step-down topology.

Power MOSFET Dissipation

Worst-case conduction losses occur at the duty-factor extremes. For the high-side MOSFET (N_H), the worst-case power dissipation due to resistance occurs at minimum input voltage:

$$PD\ (N_H\ \text{Resistive}) = \left(\frac{V_{OUT}}{V_{IN}}\right)(I_{LOAD})^2 R_{DS(ON)}$$

Generally, use a small high-side MOSFET to reduce switching losses at high input voltages. However, the $R_{DS(ON)}$ required to stay within package power-dissipation limits often limits how small the MOSFET can be. The optimum occurs when the switching losses equal the conduction ($R_{DS(ON)}$) losses. High-side switching losses do not become an issue until the input is greater than approximately 15V.

Calculating the power dissipation in high-side MOSFETs (N_H) due to switching losses is difficult since it must allow for difficult-to-quantify factors that influence the turn-on and turn-off times. These factors include the internal gate resistance, gate charge, threshold voltage, source inductance, and PC-board-layout characteristics. The following switching loss calculation provides only a very rough estimate and is no substitute for breadboard evaluation, preferably including verification using a thermocouple mounted on N_H:

$$PD\ (N_H\ \text{Switching}) = \frac{(V_{IN(MAX)})^2 C_{RSS} f_{SW} I_{LOAD}}{I_{GATE}}$$

where C_{RSS} is the reverse transfer capacitance of N_H, and I_{GATE} is the peak gate-drive source/sink current (1A typ).

Switching losses in the high-side MOSFET can become a heat problem when maximum AC-adapter voltages are applied, due to the squared term in the switching-loss equation ($C \times V_{IN}^2 \times f_{SW}$). If the high-side MOSFET chosen for adequate $R_{DS(ON)}$ at low battery voltages becomes extraordinarily hot when subjected to $V_{IN(MAX)}$, consider choosing another MOSFET with lower parasitic capacitance.

For the low-side MOSFET (N_L), the worst-case power dissipation always occurs at maximum battery voltage:

$$PD\ (N_L\ \text{Resistive}) = \left[1 - \left(\frac{V_{OUT}}{V_{IN(MAX)}}\right)\right](I_{LOAD})^2 R_{DS(ON)}$$

The absolute worst case for MOSFET power dissipation occurs under heavy overload conditions that are greater than $I_{LOAD(MAX)}$ but are not high enough to exceed the current limit and cause the fault latch to trip. To protect against this possibility, "overdesign" the circuit to tolerate:

$$I_{LOAD} = I_{LIM} - \left(\frac{I_{LOAD(MAX)} LIR}{2} \right)$$

where I_{LIM} is the peak current allowed by the current-limit circuit, including threshold tolerance and sense-resistance variation. The MOSFETs must have a relatively large heatsink to handle the overload power dissipation.

Choose a Schottky diode (D_L) with a forward-voltage drop low enough to prevent the low-side MOSFET's body diode from turning on during the dead time. As a general rule, select a diode with a DC current rating equal to 1/3rd the load current. This diode is optional and can be removed if efficiency is not critical.

Boost Capacitors

The boost capacitors (C_{BST}) must be selected large enough to handle the gate-charging requirements of the high-side MOSFETs. Typically, 0.1µF ceramic capacitors work well for low-power applications driving medium-sized MOSFETs. However, high-current applications driving large, high-side MOSFETs require boost capacitors larger than 0.1µF. For these applications, select the boost capacitors to avoid discharging the capacitor more than 200mV while charging the high-side MOSFETs' gates:

$$C_{BST} = \frac{N \times Q_{GATE}}{200mV}$$

where N is the number of high-side MOSFETs used for one regulator, and Q_{GATE} is the gate charge specified in the MOSFET's data sheet. For example, assume one IRF7811W N-channel MOSFET is used on the high side. According to the manufacturer's data sheet, a single IRF7811W has a maximum gate charge of 24nC (V_{GS} = 5V). Using the above equation, the required boost capacitance is:

$$C_{BST} = \frac{1 \times 24nC}{200mV} = 0.12\mu F$$

Selecting the closest standard value, this example requires a 0.1µF ceramic capacitor.

Applications Information

Duty-Cycle Limits

Minimum Input Voltage

The minimum input operating voltage (dropout voltage) is restricted by the maximum duty-cycle specification (see the *Electrical Characteristics* table). However, keep in mind that the transient performance gets worse as the step-down regulators approach the dropout voltage, so bulk output capacitance must be added (see the voltage sag and soar equations in the *Design Procedure* section). The absolute point of dropout occurs when the inductor current ramps down during the off-time (ΔI_{DOWN}) as much as it ramps up during the on-time (ΔI_{UP}). This results in a minimum operating voltage defined by the following equation:

$$V_{IN(MIN)} = V_{OUT} + V_{CHG} + h\left(\frac{1}{D_{MAX}} - 1 \right) (V_{OUT} + V_{DIS})$$

where V_{CHG} and V_{DIS} are the parasitic voltage drops in the charge and discharge paths, respectively. A reasonable minimum value for h is 1.5, while the absolute minimum input voltage is calculated with h = 1.

Maximum Input Voltage

The MAX1549 controller includes a minimum on-time specification, which determines the maximum input operating voltage that maintains the selected switching frequency (see the *Electrical Characteristics* table). Operation above this maximum input voltage results in pulse-skipping operation, regardless of the operating mode selected by $\overline{SKIP}$. At the beginning of each cycle, if the output voltage is still above the feedback-threshold voltage, the controller does not trigger an on-time pulse, effectively skipping a cycle. This allows the controller to maintain regulation above the maximum input voltage, but forces the controller to effectively operate with a lower switching frequency. This results in an input-threshold voltage at which the controller begins to skip pulses ($V_{IN(SKIP)}$):

$$V_{IN(SKIP)} = V_{OUT} \left(\frac{1}{f_{OSC} t_{ON(MIN)}} \right)$$

where f_{OSC} is the switching frequency selected by FSEL.

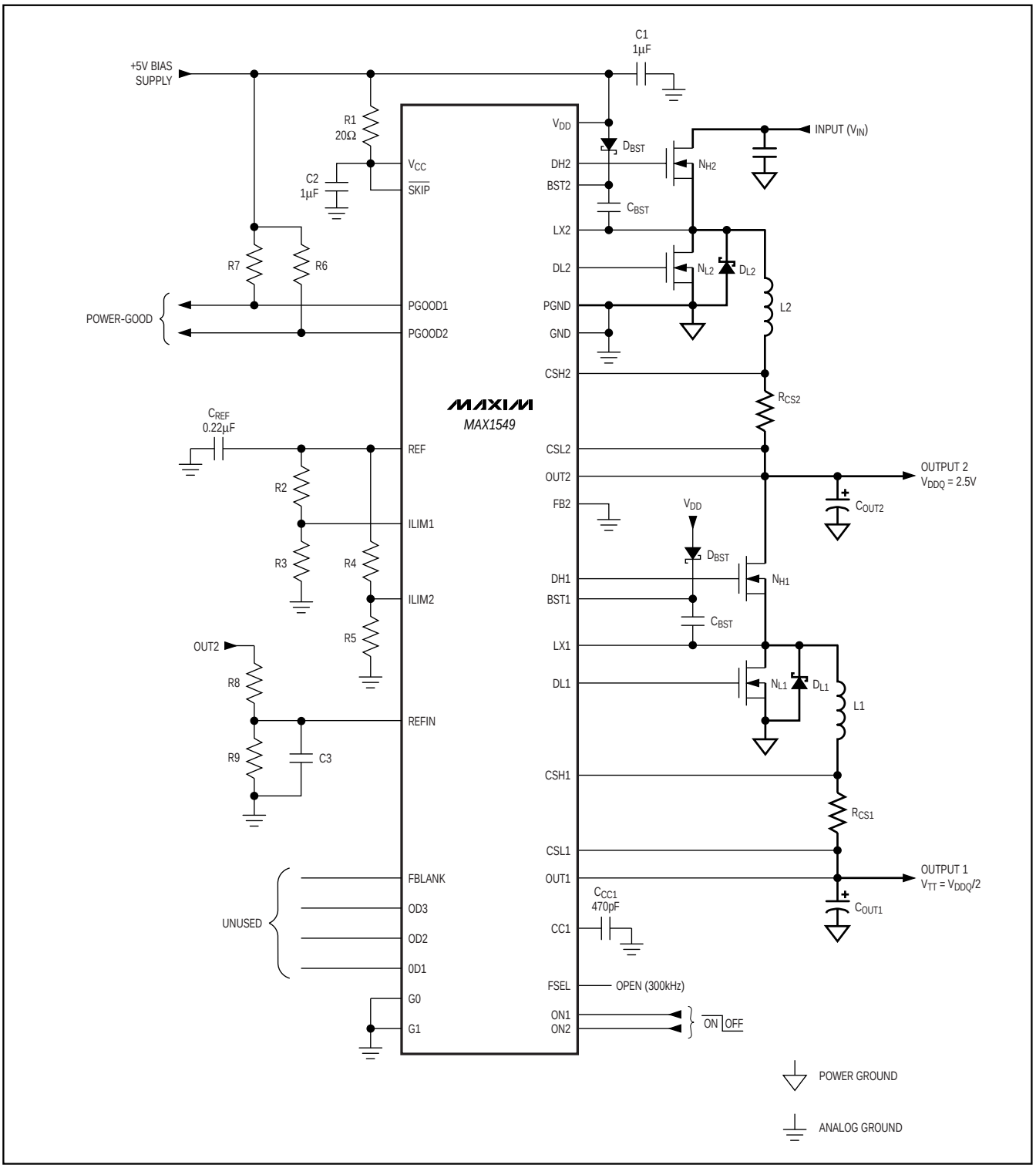


Figure 9. Active Bus Termination

Dual, Interleaved, Fixed-Frequency Step-Down Controller with a Dynamically Adjustable Output

Active Bus Termination (OUT1)

Active-bus-termination power supplies generate a voltage rail that tracks a set reference. They are required to source and sink current. DDR memory architecture requires active bus termination. In DDR memory architecture, the termination voltage is set at exactly 1/2 the memory supply voltage. Configure the main MAX1549 controller (OUT1) to generate the termination voltage using a resistive voltage-divider at REFIN. In such an application, OUT1 must be kept in PWM mode ($\overline{SKIP}$ = V_{CC} or open) for it to source and sink current. Figure 9 shows OUT1 configured as a DDR termination regulator. Connect GATE and FBLANK to GND when unused.

Voltage Positioning

Powering new mobile processors (CPU or GPU) requires careful attention to detail to reduce cost, size, and power dissipation. As processors consume more power, it was recognized that even the fastest DC-DC converters were inadequate to handle the severe transient power requirements. After a load transient, the output instantly changes by $ESR_{COUT} \times \Delta I_{LOAD}$. Conventional DC-DC converters respond by regulating the output voltage back to its nominal state after the load transient occurs (Figure 11), but the processor only requires that the output voltage remains above a specified minimum value. Dynamically positioning the output voltage to this lower limit allows the use of fewer output capacitors and reduces the power consumption under load.

Figure 10 shows the connection of OUT_ and FB_ in voltage-positioned and nonvoltage-positioned circuits. In nonvoltage-positioned circuits, the MAX1549 regulates the voltage across the output capacitor. In voltage-positioned circuits, the MAX1549 regulates the voltage on the inductor side of the current-sense resistor. The voltage-positioned output voltage is reduced to:

$$V_{OUT(VPS)} = V_{OUT(NO\ LOAD)} - R_{SENSE}I_{LOAD}$$

For a conventional (nonvoltage-positioned) circuit, the peak-to-peak voltage change is:

$$\Delta V_{OUT(CONV)} = 2 \times (ESR_{COUT} \times \Delta I_{LOAD}) + V_{SAG} + V_{SOAR}$$

where V_{SAG} and V_{SOAR} are defined in Figure 11. Setting the converter to regulate at a lower voltage when under load allows a larger voltage step when the output current suddenly decreases. Therefore, the peak-to-peak voltage change for a voltage-positioned circuit is:

$$\Delta V_{OUT(VPS)} = (ESR_{COUT} \times \Delta I_{LOAD}) + V_{SAG} + V_{SOAR}$$

where V_{SAG} and V_{SOAR} are defined in the *Design Procedure* section. Since the amplitudes are the same for both circuits ($\Delta V_{OUT(CONV)} = \Delta V_{OUT(VPS)}$), the voltage-positioned circuit tolerates twice the ESR. Since the ESR specification is achieved by paralleling several capacitors, fewer units are needed for the voltage-positioned circuit.

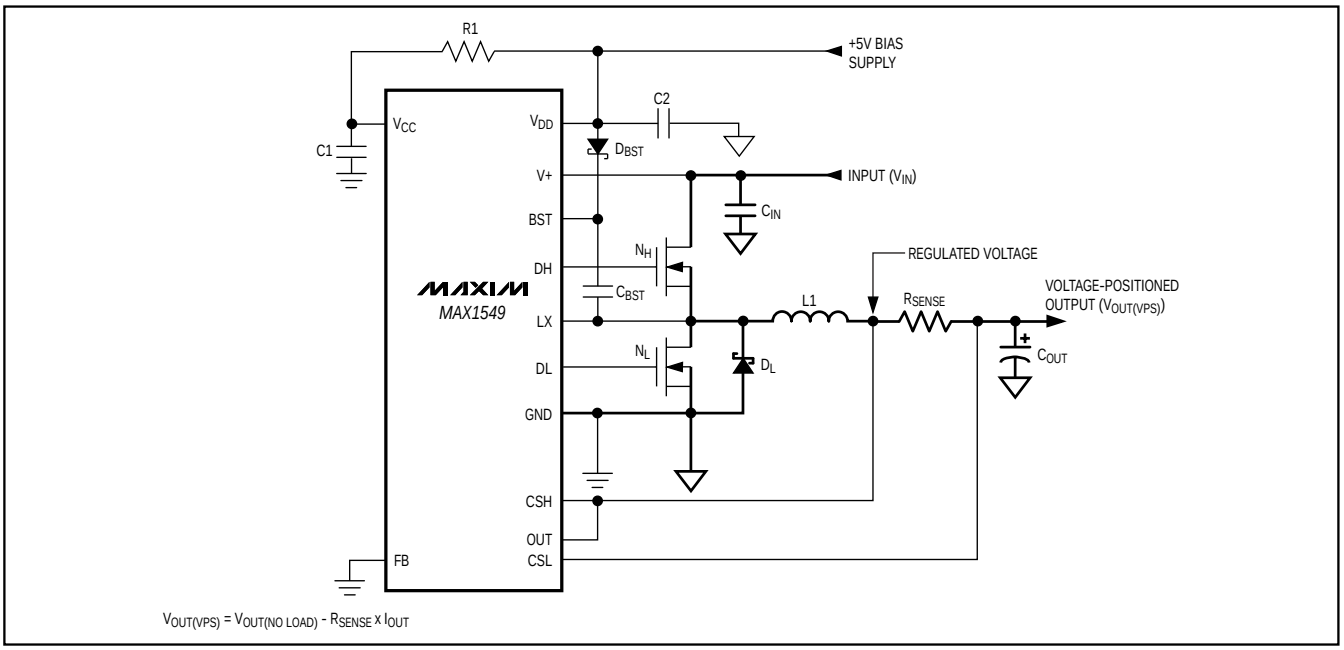


Figure 10. Voltage-Positioned Applications Circuit

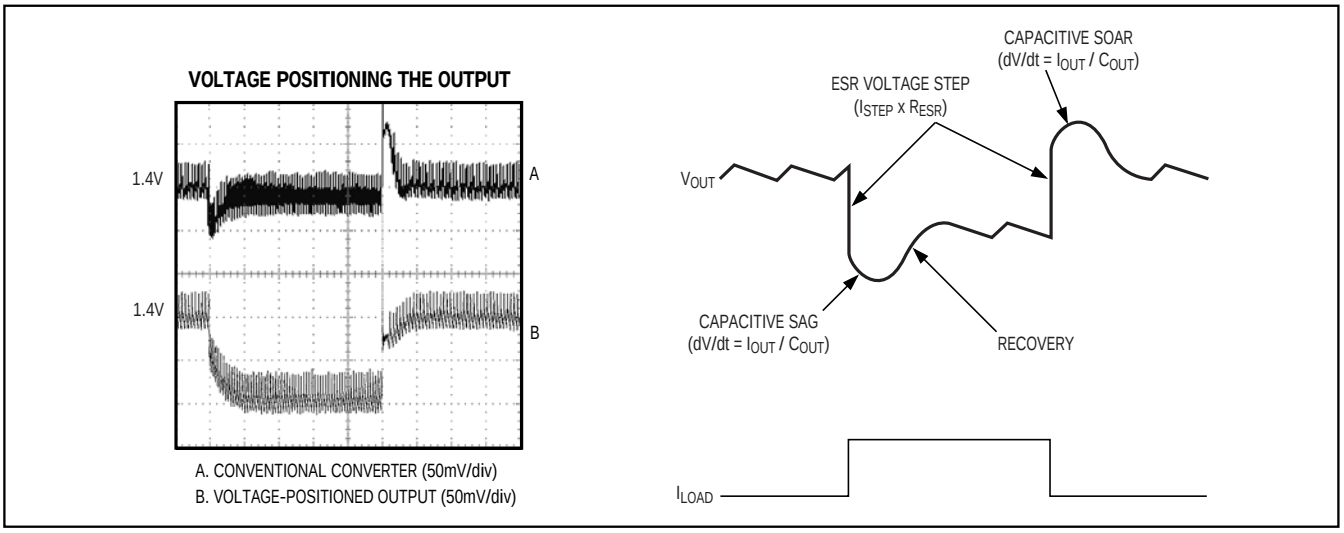


Figure 11. Voltage-Positioning Transient Response

An additional benefit of voltage positioning is reduced power consumption at high load currents. Since the output voltage is lower under load, the processor draws less current. The result is lower power dissipation in the processor, although extra power is dissipated in the current-sense element. However, the current-sense element used for current-limit protection can also be used for voltage positioning, further reducing the overall power dissipation. In effect, the processor's power dissipation is saved and the power supply dissipates some of the savings, but both the net savings and the transfer of dissipation away from the hot processor are beneficial.

PC Board Layout Guidelines

Careful PC board layout is critical to achieving low switching losses and clean, stable operation. The switching power stage requires particular attention (Figure 12). If possible, mount all the power components on the top side of the board, with their ground terminals flush against one another. Refer to the MAX1549 evaluation kit data sheet for a specific layout example. Follow these guidelines for good PC board layout:

- Use a star-ground connection on the power ground plane to minimize the crosstalk between OUT1 and OUT2.
- Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable, jitter-free operation.
- Keep the power traces and load connections short. This practice is essential for high efficiency. Using thick copper PC boards (2oz vs. 1oz) can enhance full-load efficiency by 1% or more. Correctly routing PC board traces is a difficult task that must be approached in terms of fractions of centimeters, where a single mΩ of excess trace resistance causes a measurable efficiency penalty.
- When tradeoffs in trace lengths must be made, it is preferable to allow the inductor charging path to be made longer than the discharge path. For example, it is better to allow some extra distance between the input capacitors and the high-side MOSFET than to allow distance between the inductor and the low-side MOSFET or between the inductor and the output filter capacitor.
- Minimize current-sensing errors by connecting CSH_ and CSL_ directly across the current-sense resistor ($R_{SENSE\_}$).
- Route all high-speed switching nodes (BST_, LX_, DH_, and DL_) away from sensitive analog areas (REF, FB_, CSH_, and CSL_).

Layout Procedure

1) Place the power components first, with ground terminals adjacent ($N_{L\_}$ source, C_{IN}, $C_{OUT\_}$, and $D_{L\_}$ anode). If possible, make all these connections on the top layer with wide, copper-filled areas.
2) Mount the controller IC adjacent to the low-side MOSFET, preferably on the back side opposite $N_{L\_}$ and $N_{H\_}$ to keep LX_, DH_, and the DL_ gate-drive lines short and wide. The DL_ and DH_ gate traces must be short and wide (50 mils to 100 mils wide if the MOSFET is 1in from the controller IC) to keep the driver impedance low and for proper adaptive dead-time sensing.

Dual, Interleaved, Fixed-Frequency Step-Down Controller with a Dynamically Adjustable Output

3) Group the gate-drive components (BST_ diode and capacitor, V_{DD} bypass capacitor) together near the controller IC.
4) Make the DC-DC controller ground connections as shown in Figures 1 and 12. These diagrams can be viewed as having two separate ground planes: power ground for the high-power components, and an analog ground plane for sensitive analog components. These separate ground planes must meet only at a single point directly at the IC. Additionally, a star-ground connection (centered at PGND) must be used on the power ground plane to minimize any crosstalk between the two controllers.
5) Connect the output power planes directly to the output-filter-capacitor positive and negative terminals with multiple vias. Place the entire DC-DC converter circuit as close to the load as is practical.

Chip Information

TRANSISTOR COUNT: 8823

PROCESS: BiCMOS

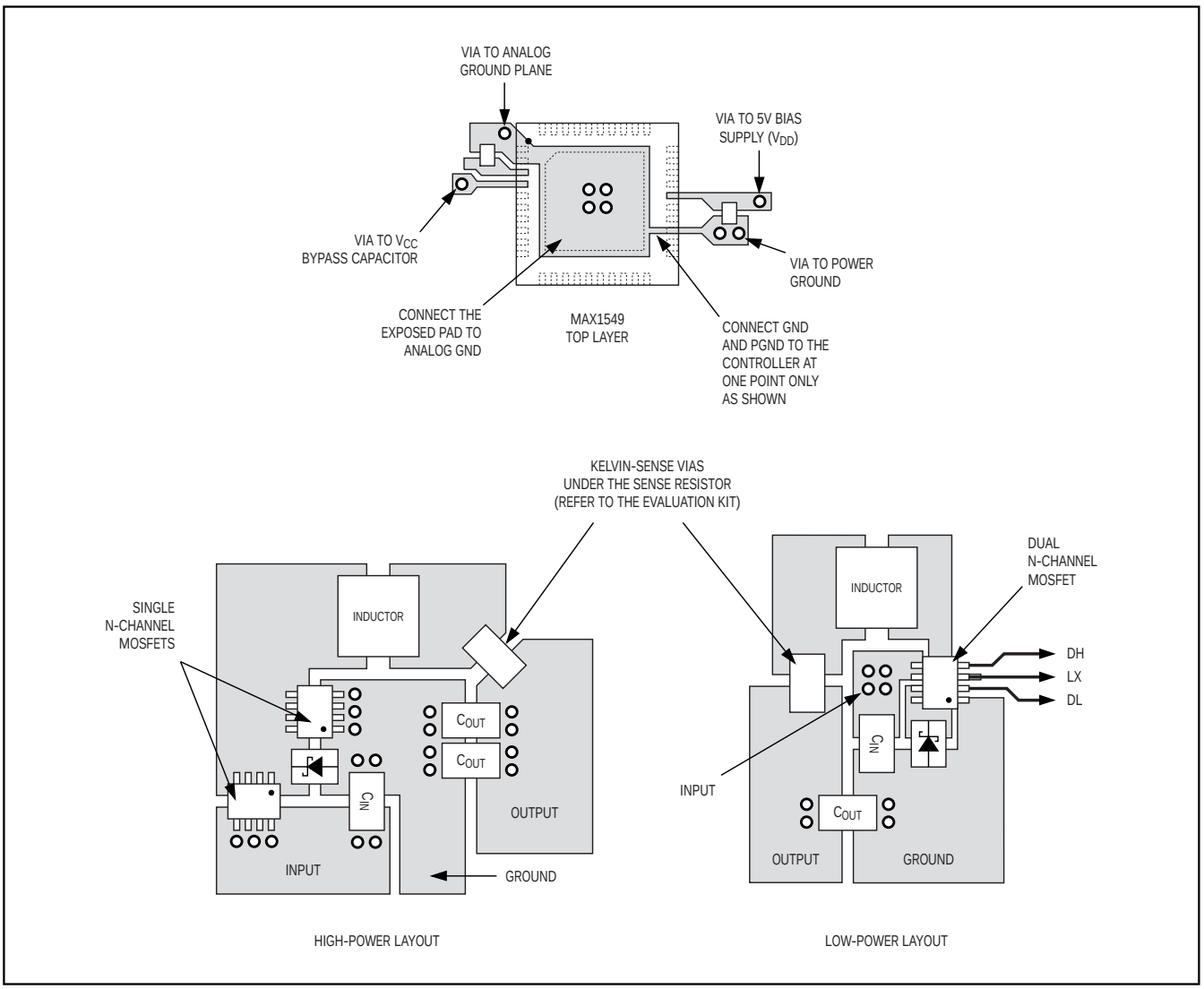
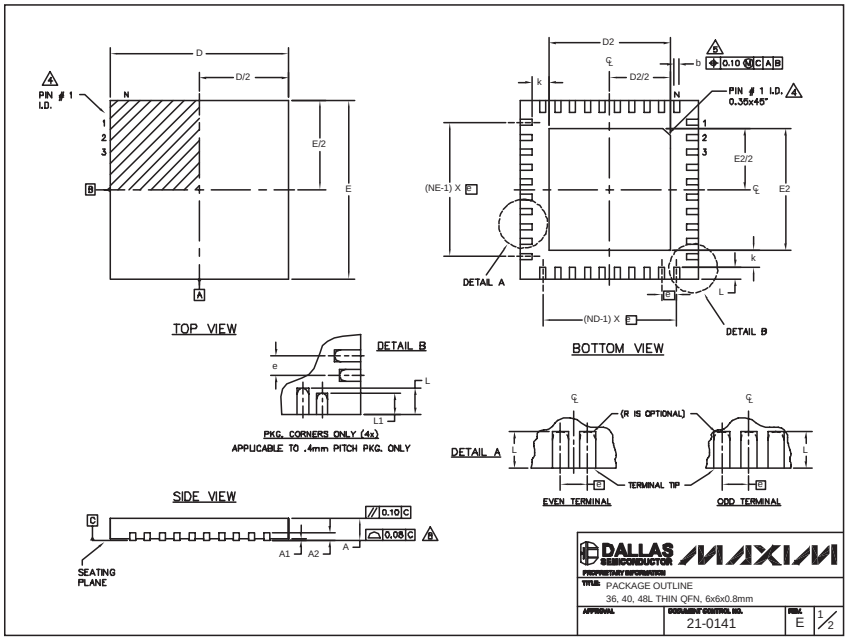


Figure 12. PC Board Layout Example

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

QFN THIN 6x6x0.8.EPS



COMMON DIMENSIONS									
PKG.	36L 6x6			40L 6x6			48L 6x6		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	–	0.05
A2	0.20 REF.			0.20 REF.			0.20 REF.		
b	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	5.90	6.00	6.10	5.90	6.00	6.10	5.90	6.00	6.10
E	5.90	6.00	6.10	5.90	6.00	6.10	5.90	6.00	6.10
e	0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	–	–	0.25	–	–	0.25	0.35	0.45
L	0.45	0.55	0.65	0.30	0.40	0.50	0.40	0.50	0.60
L1	–	–	–	–	–	–	0.30	0.40	0.50
N	36			40			48		
ND	9			10			12		
NE	9			10			12		
JEDEC	WJJD-1			WJJD-2			–		

EXPOSED PAD VARIATIONS							DOWN BONDS ALLOWED
PKG. CODES	D2			E2			
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
T3666-1	3.60	3.70	3.80	3.60	3.70	3.80	NO
T3666-2	3.60	3.70	3.80	3.60	3.70	3.80	YES
T3666-3	3.60	3.70	3.80	3.60	3.70	3.80	NO
T4066-1	4.00	4.10	4.20	4.00	4.10	4.20	NO
T4066-2	4.00	4.10	4.20	4.00	4.10	4.20	YES
T4066-3	4.00	4.10	4.20	4.00	4.10	4.20	YES
T4066-4	4.00	4.10	4.20	4.00	4.10	4.20	NO
T4066-5	4.00	4.10	4.20	4.00	4.10	4.20	NO
T4866-1	4.20	4.30	4.40	4.20	4.30	4.40	YES

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR 0.4mm LEAD PITCH PACKAGE T4866-1.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE
36, 40, 48L THIN QFN, 6x6x0.8mm
APPROVAL
DOCUMENT CONTROL NO. 21-0141
REV. E
2/2